

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				2 *****
				3 *
				4 * Zvector E7 instruction tests for VRI-d encoded:
				5 *
				6 * E772 VERIM - Vector Element Rotate and Insert Under Mask
				7 *
				8 * James Wekel April 2025
				9 *****
				11 *****
				12 *
				13 * basic instruction tests
				14 *
				15 *****
				16 * This program tests proper functioning of the z/arch E7 VRI-d
				17 * Vector Element Rotate and Insert Under Mask instruction.
				18 *
				19 * Exceptions are not tested.
				20 *
				21 * PLEASE NOTE that the tests are very SIMPLE TESTS designed to catch
				22 * obvious coding errors. None of the tests are thorough. They are
				23 * NOT designed to test all aspects of any of the instructions.
				24 *
				25 *****
				26 *
				27 * *Testcase zvector-e7-27-VERIM
				28 * *
				29 * * Zvector E7 instruction tests for VRI-d encoded:
				30 * *
				31 * * E772 VERIM - Vector Element Rotate and Insert Under Mask
				32 * *
				33 * * # -----
				34 * * # This tests only the basic function of the instructions.
				35 * * # Exceptions are NOT tested.
				36 * * # -----
				37 * *
				38 * main size 2
				39 * numcpu 1
				40 * sysclear
				41 * archlvl z/Arch
				42 *
				43 * loadcore "\$(testpath)/zvector-e7-27-VERIM core" 0x0
				44 *
				45 * diag8cmd enable # (needed for messages to Hercules console)
				46 * runtest 2
				47 * diag8cmd disable # (reset back to default)
				48 *
				49 * *Done
				50 *
				51 *
				52 *****

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				54 *****
				55 * FCHECK Macro - Is a Facility Bit set?
				56 *
				57 * If the facility bit is NOT set, an message is issued and
				58 * the test is skipped.
				59 *
				60 * Fcheck uses R0, R1 and R2
				61 *
				62 * eg. FCHECK 134, 'vector-packed-decimal'
				63 *****
				64 MACRO
				65 FCHECK &BITNO, &NOTSETMSG
				66 . * &BITNO : facility bit number to check
				67 . * &NOTSETMSG : 'facility name'
				68 LCLA &FBBYTE Facility bit in Byte
				69 LCLA &FBBIT Facility bit within Byte
				70
				71 LCLA &L(8)
				72 &L(1) SetA 128, 64, 32, 16, 8, 4, 2, 1 bit positions within byte
				73
				74 &FBBYTE SETA &BITNO/8
				75 &FBBIT SETA &L((&BITNO-(&FBBYTE*8))+1)
				76 . * MNOTE 0, 'checking Bit=&BITNO: FBBYTE=&FBBYTE, FBBIT=&FBBIT'
				77
				78 B X&SYSNDX
				79 * Fcheck data area
				80 * skip messgae
				81 SKT&SYSNDX DC C' Skipping tests: '
				82 DC C&NOTSETMSG
				83 DC C' (bit &BITNO) is not installed.'
				84 SKL&SYSNDX EQU *-SKT&SYSNDX
				85 * facility bits
				86 DS FD gap
				87 FB&SYSNDX DS 4FD
				88 DS FD gap
				89 *
				90 X&SYSNDX EQU *
				91 LA R0, ((X&SYSNDX- FB&SYSNDX)/8)-1
				92 STFLE FB&SYSNDX get facility bits
				93
				94 XGR R0, R0
				95 IC R0, FB&SYSNDX+&FBBYTE get fbit byte
				96 N R0, =F' &FBBIT' is bit set?
				97 BNZ XC&SYSNDX
				98 *
				99 * facility bit not set, issue message and exit
				100 *
				101 LA R0, SKL&SYSNDX message length
				102 LA R1, SKT&SYSNDX message address
				103 BAL R2, MSG
				104
				105 B EOJ
				106 XC&SYSNDX EQU *
				107 MEND

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				109	*****
				110	* Low core PSWs
				111	*****
00000000		00000000	0000497B	112	ZVE7TST START 0
		00000000		113	USING ZVE7TST, R0 Low core addressability
		00000140	00000000	114	
				115	SVOLDPSW EQU ZVE7TST+X' 140' z/Arch Supervisor call old PSW
00000000		00000000	000001A0	117	ORG ZVE7TST+X' 1A0' z/Architecture RESTART PSW
000001A0	00000001 80000000			118	DC X' 0000000180000000'
000001A8	00000000 00000200			119	DC AD(BEGIN)
000001B0		000001B0	000001D0	121	ORG ZVE7TST+X' 1D0' z/Architecture PROGRAM CHECK PSW
000001D0	00020001 80000000			122	DC X' 0002000180000000'
000001D8	00000000 0000DEAD			123	DC AD(X' DEAD')
000001E0		000001E0	00000200	125	ORG ZVE7TST+X' 200' Start of actual test program..
				127	*****
				128	* The actual "ZVE7TST" program itself...
				129	*****
				130	*
				131	* Architecture Mode: z/Arch
				132	* Register Usage:
				133	*
				134	* R0 (work)
				135	* R1- 4 (work)
				136	* R5 Testing control table - current test base
				137	* R6- R7 (work)
				138	* R8 First base register
				139	* R9 Second base register
				140	* R10 Third base register
				141	* R11 E7TEST call return
				142	* R12 E7TESTS register
				143	* R13 (work)
				144	* R14 Subroutine call
				145	* R15 Secondary Subroutine call or work
				146	*
				147	*****
00000200		00000200		149	USING BEGIN, R8 FIRST Base Register
00000200		00001200		150	USING BEGIN+4096, R9 SECOND Base Register
00000200		00002200		151	USING BEGIN+8192, R10 THIRD Base Register
00000200	0580			153	BEGIN BALR R8, 0 Inititalize FIRST base register
00000202	0680			154	BCTR R8, 0 Inititalize FIRST base register
00000204	0680			155	BCTR R8, 0 Inititalize FIRST base register
00000206	4190 8800		00000800	157	LA R9, 2048(, R8) Inititalize SECOND base register
0000020A	4190 9800		00000800	158	LA R9, 2048(, R9) Inititalize SECOND base register
				159	

[illegible]

LOC	OBJECT CODE		ADDR1	ADDR2	STMT			
					255	*****		
					256	*	RPTERROR	Report instruction test in error
					257	*****		
0000032C	50F0	81AC		000003AC	259	RPTERROR	ST	R15, RPTSAVE Save return address
00000330	5050	81B0		000003B0	260		ST	R5, RPTSVR5 Save R5
					261	*		
00000334	4820	5004		00000004	262		LH	R2, TNUM get test number and convert
00000338	4E20	8E80		00001080	263		CVD	R2, DECNUM
0000033C	D211	8E6A 8E54	0000106A	00001054	264		MVC	PRT3, EDIT
00000342	DE11	8E6A 8E80	0000106A	00001080	265		ED	PRT3, DECNUM
00000348	D202	8E18 8E77	00001018	00001077	266		MVC	PRTNUM(3), PRT3+13 fill in message with test #
					267			
0000034E	D207	8E33 5009	00001033	00000009	268		MVC	PRTNAME, OPNAME fill in message with instruction
					269			
00000354	1722				270		XR	R2, R2
00000356	4320	5007		00000007	271		IC	R2, i4 get i4 and convert
0000035A	4E20	8E80		00001080	272		CVD	R2, DECNUM
0000035E	D211	8E6A 8E54	0000106A	00001054	273		MVC	PRT3, EDIT
00000364	DE11	8E6A 8E80	0000106A	00001080	274		ED	PRT3, DECNUM
0000036A	D202	8E44 8E77	00001044	00001077	275		MVC	PRTI4(3), PRT3+13 fill in message with i4 field
					276			
00000370	1722				277		XR	R2, R2
00000372	4320	5008		00000008	278		IC	R2, m5 get m5 and convert
00000376	4E20	8E80		00001080	279		CVD	R2, DECNUM
0000037A	D211	8E6A 8E54	0000106A	00001054	280		MVC	PRT3, EDIT
00000380	DE11	8E6A 8E80	0000106A	00001080	281		ED	PRT3, DECNUM
00000386	D201	8E51 8E78	00001051	00001078	282		MVC	PRTM5(2), PRT3+14 fill in message with i4 field
					283	*		
					284	*		
					285	*		
0000038C	9002	81B8		000003B8	286		STM	R0, R2, RPTDWSAV save regs used by MSG
00000390	4100	004C		0000004C	287		LA	R0, PRTLNG message length
00000394	4110	8E08		00001008	288		LA	R1, PRTLNE messagfe address
00000398	4520	81C8		000003C8	289		BAL	R2, MSG call Hercules console MSG display
0000039C	9802	81B8		000003B8	290		LM	R0, R2, RPTDWSAV restore regs
000003A0	5850	81B0		000003B0	292		L	R5, RPTSVR5 Restore R5
000003A4	58F0	81AC		000003AC	293		L	R15, RPTSAVE Restore return address
000003A8	07FF				294		BR	R15 Return to caller
000003AC	00000000				296	RPTSAVE	DC	F' 0' R15 save area
000003B0	00000000				297	RPTSVR5	DC	F' 0' R5 save area
000003B8	00000000	00000000			299	RPTDWSAV	DC	2D' 0' R0-R2 save area for MSG call

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
				340 *****
				341 * Normal completion or Abnormal termination PSWs
				342 *****
00000480	00020001 80000000			344 E0JPSW DC 0D' 0' , X' 0002000180000000' , AD(0)
00000490	B2B2 8280		00000480	346 E0J LPSWE E0JPSW Normal completion
00000498	00020001 80000000			348 FAILPSW DC 0D' 0' , X' 0002000180000000' , AD(X' BAD')
000004A8	B2B2 8298		00000498	350 FAILTEST LPSWE FAILPSW Abnormal termination
				352 *****
				353 * Working Storage
				354 *****
000004AC	00000000			356 CTLR0 DS F CRO
000004B0	00000000			357 DS F
000004B4				359 LTORG , Literals pool
000004B4	00000040			360 =F' 64'
000004B8	00004844			361 =A(E7TESTS)
000004BC	00000001			362 =F' 1'
000004C0	0000			363 =H' 0'
000004C2	005F			364 =AL2(L' MSGMSG)
				365
				366 * some constants
				367
	00000400	00000001		368 K EQU 1024 One KB
	00001000	00000001		369 PAGE EQU (4*K) Size of one page
	00010000	00000001		370 K64 EQU (64*K) 64 KB
	00100000	00000001		371 MB EQU (K*K) 1 MB
				372
	AABBCCDD	00000001		373 REG2PATT EQU X' AABBCCDD' Polluted Register pattern
	000000DD	00000001		374 REG2LOW EQU X' DD' (last byte above)

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				419	*****
				420	* E7TEST DSECT
				421	*****
				423	E7TEST DSECT ,
00000000	00000000			424	TSUB DC A(0) pointer to test
00000004	0000			425	TNUM DC H' 00' Test Number
00000006	00			426	DC X' 00'
00000007	00			427	I4 DC HL1' 00' i4 field
00000008	00			428	M5 DC HL1' 00' m5 field
				429	
00000009	40404040	40404040		430	OPNAME DC CL8' ' E7 name
00000014	00000000			431	V1ADDR DC A(0) address of v1 source
00000018	00000000			432	V2ADDR DC A(0) address of v2 source
0000001C	00000000			433	V3ADDR DC A(0) address of v3 source
00000020	00000000			434	RELEN DC A(0) RESULT LENGTH
00000024	00000000			435	READDR DC A(0) result (expected) address
00000028	00000000	00000000		436	DS FD gap
00000030	00000000	00000000		437	V10OUTPUT DS XL16 V1 Output
00000040	00000000	00000000		438	DS FD gap
				439	
				440	* test routine will be here (from VRI-d macro)
				441	*
				442	* followed by
				443	* EXPECTED RESULT
				445	ZVE7TST CSECT ,
000010C0		00000000	0000497B	446	DS 0F
				448	*****
				449	* Macros to help build test tables
				450	*****
				452	*
				453	* macro to generate individual test
				454	*
				455	MACRO
				456	VRI_D &INST, &I4, &M5
				457	. * &INST - VRI-d instruction under test
				458	. * &I4 - rotate shift
				459	. * &M5 - element size
				460	
				461	GBLA &TNUM
				462	&TNUM SETA &TNUM+1
				463	
				464	DS 0FD
				465	USING *, R5 base for test data and test routine
				466	
				467	T&TNUM DC A(X&TNUM) address of test routine
				468	DC H' &TNUM test number
				469	DC X' 00'

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				470	DC	HL1' &I4'	i4 field
				471	DC	HL1' &M5'	m5 field
				472	DC	CL8' &INST'	instruction name
				473	DC	A(RE&TNUM+16)	address of v1 source
				474	DC	A(RE&TNUM+32)	address of v2 source
				475	DC	A(RE&TNUM+48)	address of v3 source
				476	DC	A(16)	result length
				477	REA&TNUM	DC A(RE&TNUM)	result address
				478	DS	FD	gap
				479	V10&TNUM	DS XL16	V1 output
				480	DS	FD	gap
				481	.	*	
				482	*		
				483	X&TNUM	DS OF	
				484	LGF	R1, V1ADDR	load v1 source
				485	VL	v21, 0(R1)	use v21 to test decoder
				486			
				487	LGF	R1, V2ADDR	load v2 source
				488	VL	v22, 0(R1)	use v22 to test decoder
				489			
				490	LGF	R1, V3ADDR	load v3 source
				491	VL	v23, 0(R1)	use v23 to test decoder
				492			
				493		&INST V21, V22, V23, &I4, &M5	test instruction
				494			
				495	VST	V21, V10&TNUM	save v1 output
				496	BR	R11	return
				497			
				498	RE&TNUM	DC OF	xl16 expected result
				499			
				500	DROP	R5	
				501	MEND		
				503	*		
				504	*	macro to generate table of pointers to individual tests	
				505	*		
				506		MACRO	
				507		PTTABLE	
				508		GBLA &TNUM	
				509		LCLA &CUR	
				510	&CUR	SETA 1	
				511	.	*	
				512	TTABLE	DS OF	
				513	. LOOP	ANOP	
				514	.	*	
				515		DC A(T&CUR)	
				516	.	*	
				517	&CUR	SETA &CUR+1	
				518	AIF	(&CUR LE &TNUM) . LOOP	
				519	*		
				520	DC	A(0)	END OF TABLE
				521	DC	A(0)	
				522	.	*	
				523		MEND	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT
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524

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				526 *****	
				527 * E7 VRI-d tests	
				528 *****	
				529 PRINT DATA	
				530	
				531 * E772 VERIM - Vector Element Rotate and Insert Under Mask	
				532	
				533 * VRI-d instruction, i4, m5	
				534 * followed by	
				535 * 16 byte expected result (V1)	
				536 * 16 byte V2 source	
				537 * 16 byte V3 source	
				538 * -----	
				539 * VERIM - Vector Element Rotate and Insert Under Mask	
				540 * -----	
				541 * -----	
				542 * case 0 - testing test	
				543 * -----	
				544 *Byte	
				545 VRI_D VERIM, 0, 0	
000010C0				546+ DS OFD	
000010C0		000010C0		547+ USING *, R5	base for test data and test routine
000010C0	00001108			548+T1 DC A(X1)	address of test routine
000010C4	0001			549+ DC H' 1'	test number
000010C6	00			550+ DC X' 00'	
000010C7	00			551+ DC HL1' 0'	i4 field
000010C8	00			552+ DC HL1' 0'	m5 field
000010C9	E5C5D9C9 D4404040			553+ DC CL8' VERIM	instruction name
000010D4	0000114C			554+ DC A(RE1+16)	address of v1 source
000010D8	0000115C			555+ DC A(RE1+32)	address of v2 source
000010DC	0000116C			556+ DC A(RE1+48)	address of v3 source
000010E0	00000010			557+ DC A(16)	result length
000010E4	0000113C			558+REA1 DC A(RE1)	result address
000010E8	00000000 00000000			559+ DS FD	gap
000010F0	00000000 00000000			560+V101 DS XL16	V1 output
000010F8	00000000 00000000				
00001100	00000000 00000000			561+ DS FD	gap
				562+*	
00001108				563+X1 DS OF	
00001108	E310 5014 0014	00000014		564+ LGF R1, V1ADDR	load v1 source
0000110E	E751 0000 0806	00000000		565+ VL v21, 0(R1)	use v21 to test decoder
00001114	E310 5018 0014	00000018		566+ LGF R1, V2ADDR	load v2 source
0000111A	E761 0000 0806	00000000		567+ VL v22, 0(R1)	use v22 to test decoder
00001120	E310 501C 0014	0000001C		568+ LGF R1, V3ADDR	load v3 source
00001126	E771 0000 0806	00000000		569+ VL v23, 0(R1)	use v23 to test decoder
0000112C	E756 7000 0E72			570+ VERIM V21, V22, V23, 0, 0	test instruction
00001132	E750 5030 080E	000010F0		571+ VST V21, V101	save v1 output
00001138	07FB			572+ BR R11	return
0000113C				573+RE1 DC OF	xl16 expected result
0000113C				574+ DROP R5	
0000113C	00010203 04050607			575 DC XL16' 0001020304050607 08090A0B0C0D0E0F'	result t
00001144	08090A0B 0C0D0E0F				
0000114C	00010203 04050607		576	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00001154	08090A0B 0C0D0E0F				
0000115C	0F0E0D0C 0B0A0908		577	DC XL16' 0F0E0D0C0B0A0908 0706050403020100'	v2
00001164	07060504 03020100				

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
0000116C	00000000 00000000			578	DC	XL16' 0000000000000000 0000000000000000'	v3	
00001174	00000000 00000000							
				579				
				580	VRI_D	VERIM, 0, 0		
00001180				581+	DS	0FD		
00001180		00001180		582+	USING	*, R5	base for test data and test routine	
00001180	000011C8			583+T2	DC	A(X2)	address of test routine	
00001184	0002			584+	DC	H' 2'	test number	
00001186	00			585+	DC	X' 00'		
00001187	00			586+	DC	HL1' 0'	i4 field	
00001188	00			587+	DC	HL1' 0'	m5 field	
00001189	E5C5D9C9 D4404040			588+	DC	CL8' VERIM	instruction name	
00001194	0000120C			589+	DC	A(RE2+16)	address of v1 source	
00001198	0000121C			590+	DC	A(RE2+32)	address of v2 source	
0000119C	0000122C			591+	DC	A(RE2+48)	address of v3 source	
000011A0	00000010			592+	DC	A(16)	result length	
000011A4	000011FC			593+REA2	DC	A(RE2)	result address	
000011A8	00000000 00000000			594+	DS	FD	gap	
000011B0	00000000 00000000			595+V102	DS	XL16	V1 output	
000011B8	00000000 00000000							
000011C0	00000000 00000000			596+	DS	FD	gap	
				597+*				
000011C8				598+X2	DS	0F		
000011C8	E310 5014 0014		00000014	599+	LGF	R1, V1ADDR	load v1 source	
000011CE	E751 0000 0806		00000000	600+	VL	v21, 0(R1)	use v21 to test decoder	
000011D4	E310 5018 0014		00000018	601+	LGF	R1, V2ADDR	load v2 source	
000011DA	E761 0000 0806		00000000	602+	VL	v22, 0(R1)	use v22 to test decoder	
000011E0	E310 501C 0014		0000001C	603+	LGF	R1, V3ADDR	load v3 source	
000011E6	E771 0000 0806		00000000	604+	VL	v23, 0(R1)	use v23 to test decoder	
000011EC	E756 7000 0E72			605+	VERIM	V21, V22, V23, 0, 0	test instruction	
000011F2	E750 5030 080E		000011B0	606+	VST	V21, V102	save v1 output	
000011F8	07FB			607+	BR	R11	return	
000011FC				608+RE2	DC	0F	xl16 expected result	
000011FC				609+	DROP	R5		
000011FC	0F0E0D0C 0B0A0908			610	DC	XL16' 0F0E0D0C0B0A0908 0706050403020100'	result t	
00001204	07060504 03020100							
0000120C	00010203 04050607			611	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00001214	08090A0B 0C0D0E0F							
0000121C	0F0E0D0C 0B0A0908			612	DC	XL16' 0F0E0D0C0B0A0908 0706050403020100'	v2	
00001224	07060504 03020100							
0000122C	FFFFFFFF FFFFFFFF			613	DC	XL16' FFFFFFFFFFFFFFFFFF FFFFFFFFFFFFFFFFFF'	v3	
00001234	FFFFFFFF FFFFFFFF							
				614				
				615	*	-----		
				616	*	case 1		
				617	*	-----		
				618	*Byte			
				619	VRI_D	VERIM, 0, 0		
00001240				620+	DS	0FD		
00001240		00001240		621+	USING	*, R5	base for test data and test routine	
00001240	00001288			622+T3	DC	A(X3)	address of test routine	
00001244	0003			623+	DC	H' 3'	test number	
00001246	00			624+	DC	X' 00'		
00001247	00			625+	DC	HL1' 0'	i4 field	
00001248	00			626+	DC	HL1' 0'	m5 field	
00001249	E5C5D9C9 D4404040			627+	DC	CL8' VERIM	instruction name	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001254	000012CC			628+	DC	A(RE3+16)	address of v1 source
00001258	000012DC			629+	DC	A(RE3+32)	address of v2 source
0000125C	000012EC			630+	DC	A(RE3+48)	address of v3 source
00001260	00000010			631+	DC	A(16)	result length
00001264	000012BC			632+REA3	DC	A(RE3)	result address
00001268	00000000 00000000			633+	DS	FD	gap
00001270	00000000 00000000			634+V103	DS	XL16	V1 output
00001278	00000000 00000000						
00001280	00000000 00000000			635+	DS	FD	gap
				636+*			
00001288				637+X3	DS	0F	
00001288	E310 5014 0014		00000014	638+	LGF	R1, V1ADDR	load v1 source
0000128E	E751 0000 0806		00000000	639+	VL	v21, 0(R1)	use v21 to test decoder
00001294	E310 5018 0014		00000018	640+	LGF	R1, V2ADDR	load v2 source
0000129A	E761 0000 0806		00000000	641+	VL	v22, 0(R1)	use v22 to test decoder
000012A0	E310 501C 0014		0000001C	642+	LGF	R1, V3ADDR	load v3 source
000012A6	E771 0000 0806		00000000	643+	VL	v23, 0(R1)	use v23 to test decoder
000012AC	E756 7000 0E72			644+	VERIM	V21, V22, V23, 0, 0	test instruction
000012B2	E750 5030 080E		00001270	645+	VST	V21, V103	save v1 output
000012B8	07FB			646+	BR	R11	return
000012BC				647+RE3	DC	0F	xl16 expected result
000012BC				648+	DROP	R5	
000012BC	F0F1F2F3 F4F5F6F7			649	DC	XL16' F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	result t
000012C4	F8F9FAFB FCFDFEFF						
000012CC	F0F0F0F0 F0F0F0F0			650	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
000012D4	F0F0F0F0 F0F0F0F0						
000012DC	00010203 04050607			651	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000012E4	08090A0B 0C0D0E0F						
000012EC	0F0F0F0F 0F0F0F0F			652	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000012F4	0F0F0F0F 0F0F0F0F						
				653			
				654	VRI_D	VERIM, 1, 0	
00001300				655+	DS	0FD	
00001300		00001300		656+	USING	*, R5	base for test data and test routine
00001300	00001348			657+T4	DC	A(X4)	address of test routine
00001304	0004			658+	DC	H' 4'	test number
00001306	00			659+	DC	X' 00'	
00001307	01			660+	DC	HL1' 1'	i4 field
00001308	00			661+	DC	HL1' 0'	m5 field
00001309	E5C5D9C9 D4404040			662+	DC	CL8' VERIM	instruction name
00001314	0000138C			663+	DC	A(RE4+16)	address of v1 source
00001318	0000139C			664+	DC	A(RE4+32)	address of v2 source
0000131C	000013AC			665+	DC	A(RE4+48)	address of v3 source
00001320	00000010			666+	DC	A(16)	result length
00001324	0000137C			667+REA4	DC	A(RE4)	result address
00001328	00000000 00000000			668+	DS	FD	gap
00001330	00000000 00000000			669+V104	DS	XL16	V1 output
00001338	00000000 00000000						
00001340	00000000 00000000			670+	DS	FD	gap
				671+*			
00001348				672+X4	DS	0F	
00001348	E310 5014 0014		00000014	673+	LGF	R1, V1ADDR	load v1 source
0000134E	E751 0000 0806		00000000	674+	VL	v21, 0(R1)	use v21 to test decoder
00001354	E310 5018 0014		00000018	675+	LGF	R1, V2ADDR	load v2 source
0000135A	E761 0000 0806		00000000	676+	VL	v22, 0(R1)	use v22 to test decoder
00001360	E310 501C 0014		0000001C	677+	LGF	R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001366	E771 0000 0806		00000000	678+	VL	v23, 0(R1)	use v23 to test decoder
0000136C	E756 7001 0E72			679+	VERIM	V21, V22, V23, 1, 0	test instruction
00001372	E750 5030 080E		00001330	680+	VST	V21, V104	save v1 output
00001378	07FB			681+	BR	R11	return
0000137C				682+RE4	DC	0F	xl16 expected result
0000137C				683+	DROP	R5	
0000137C	F0F2F4F6 F8FAFCFE			684	DC	XL16' F0F2F4F6F8FAFCFE F0F2F4F6F8FAFCFE'	result t
00001384	F0F2F4F6 F8FAFCFE						
0000138C	F0F0F0F0 F0F0F0F0			685	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001394	F0F0F0F0 F0F0F0F0						
0000139C	00010203 04050607			686	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000013A4	08090A0B 0C0D0E0F						
000013AC	0F0F0F0F 0F0F0F0F			687	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000013B4	0F0F0F0F 0F0F0F0F						
				688			
				689	VRI_D	VERIM, 2, 0	
000013C0				690+	DS	0FD	
000013C0		000013C0		691+	USING	*, R5	base for test data and test routine
000013C0	00001408			692+T5	DC	A(X5)	address of test routine
000013C4	0005			693+	DC	H' 5'	test number
000013C6	00			694+	DC	X' 00'	
000013C7	02			695+	DC	HL1' 2'	i4 field
000013C8	00			696+	DC	HL1' 0'	m5 field
000013C9	E5C5D9C9 D4404040			697+	DC	CL8' VERIM	instruction name
000013D4	0000144C			698+	DC	A(RE5+16)	address of v1 source
000013D8	0000145C			699+	DC	A(RE5+32)	address of v2 source
000013DC	0000146C			700+	DC	A(RE5+48)	address of v3 source
000013E0	00000010			701+	DC	A(16)	result length
000013E4	0000143C			702+REA5	DC	A(RE5)	result address
000013E8	00000000 00000000			703+	DS	FD	gap
000013F0	00000000 00000000			704+V105	DS	XL16	V1 output
000013F8	00000000 00000000						
00001400	00000000 00000000			705+	DS	FD	gap
				706+*			
00001408				707+X5	DS	0F	
00001408	E310 5014 0014		00000014	708+	LGF	R1, V1ADDR	load v1 source
0000140E	E751 0000 0806		00000000	709+	VL	v21, 0(R1)	use v21 to test decoder
00001414	E310 5018 0014		00000018	710+	LGF	R1, V2ADDR	load v2 source
0000141A	E761 0000 0806		00000000	711+	VL	v22, 0(R1)	use v22 to test decoder
00001420	E310 501C 0014		0000001C	712+	LGF	R1, V3ADDR	load v3 source
00001426	E771 0000 0806		00000000	713+	VL	v23, 0(R1)	use v23 to test decoder
0000142C	E756 7002 0E72			714+	VERIM	V21, V22, V23, 2, 0	test instruction
00001432	E750 5030 080E		000013F0	715+	VST	V21, V105	save v1 output
00001438	07FB			716+	BR	R11	return
0000143C				717+RE5	DC	0F	xl16 expected result
0000143C				718+	DROP	R5	
0000143C	F0F4F8FC F0F4F8FC			719	DC	XL16' F0F4F8FCF0F4F8FC F0F4F8FCF0F4F8FC'	result t
00001444	F0F4F8FC F0F4F8FC						
0000144C	F0F0F0F0 F0F0F0F0			720	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001454	F0F0F0F0 F0F0F0F0						
0000145C	00010203 04050607			721	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001464	08090A0B 0C0D0E0F						
0000146C	0F0F0F0F 0F0F0F0F			722	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001474	0F0F0F0F 0F0F0F0F						
				723			
				724	VRI_D	VERIM, 5, 0	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001480				725+	DS	OFD	
00001480		00001480		726+	USING	*, R5	base for test data and test routine
00001480	000014C8			727+T6	DC	A(X6)	address of test routine
00001484	0006			728+	DC	H' 6'	test number
00001486	00			729+	DC	X' 00'	
00001487	05			730+	DC	HL1' 5'	i4 field
00001488	00			731+	DC	HL1' 0'	m5 field
00001489	E5C5D9C9 D4404040			732+	DC	CL8' VERIM	instruction name
00001494	0000150C			733+	DC	A(RE6+16)	address of v1 source
00001498	0000151C			734+	DC	A(RE6+32)	address of v2 source
0000149C	0000152C			735+	DC	A(RE6+48)	address of v3 source
000014A0	00000010			736+	DC	A(16)	result length
000014A4	000014FC			737+REA6	DC	A(RE6)	result address
000014A8	00000000 00000000			738+	DS	FD	gap
000014B0	00000000 00000000			739+V106	DS	XL16	V1 output
000014B8	00000000 00000000						
000014C0	00000000 00000000			740+	DS	FD	gap
				741+*			
000014C8				742+X6	DS	OF	
000014C8	E310 5014 0014		00000014	743+	LGF	R1, V1ADDR	load v1 source
000014CE	E751 0000 0806		00000000	744+	VL	v21, 0(R1)	use v21 to test decoder
000014D4	E310 5018 0014		00000018	745+	LGF	R1, V2ADDR	load v2 source
000014DA	E761 0000 0806		00000000	746+	VL	v22, 0(R1)	use v22 to test decoder
000014E0	E310 501C 0014		0000001C	747+	LGF	R1, V3ADDR	load v3 source
000014E6	E771 0000 0806		00000000	748+	VL	v23, 0(R1)	use v23 to test decoder
000014EC	E756 7005 0E72			749+	VERIM	V21, V22, V23, 5, 0	test instruction
000014F2	E750 5030 080E		000014B0	750+	VST	V21, V106	save v1 output
000014F8	07FB			751+	BR	R11	return
000014FC				752+RE6	DC	OF	xl16 expected result
000014FC				753+	DROP	R5	
000014FC	F0F0F0F0 F0F0F0F0			754	DC	XL16' F0F0F0F0F0F0F0F0 F1F1F1F1F1F1F1F1'	result t
00001504	F1F1F1F1 F1F1F1F1						
0000150C	F0F0F0F0 F0F0F0F0			755	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001514	F0F0F0F0 F0F0F0F0						
0000151C	00010203 04050607			756	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001524	08090A0B 0C0D0E0F						
0000152C	0F0F0F0F 0F0F0F0F			757	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001534	0F0F0F0F 0F0F0F0F						
				758			
				759	VRI_D	VERIM, 7, 0	
00001540				760+	DS	OFD	
00001540		00001540		761+	USING	*, R5	base for test data and test routine
00001540	00001588			762+T7	DC	A(X7)	address of test routine
00001544	0007			763+	DC	H' 7'	test number
00001546	00			764+	DC	X' 00'	
00001547	07			765+	DC	HL1' 7'	i4 field
00001548	00			766+	DC	HL1' 0'	m5 field
00001549	E5C5D9C9 D4404040			767+	DC	CL8' VERIM	instruction name
00001554	000015CC			768+	DC	A(RE7+16)	address of v1 source
00001558	000015DC			769+	DC	A(RE7+32)	address of v2 source
0000155C	000015EC			770+	DC	A(RE7+48)	address of v3 source
00001560	00000010			771+	DC	A(16)	result length
00001564	000015BC			772+REA7	DC	A(RE7)	result address
00001568	00000000 00000000			773+	DS	FD	gap
00001570	00000000 00000000			774+V107	DS	XL16	V1 output
00001578	00000000 00000000						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001580	00000000 00000000			775+ 776+*	DS	FD	gap
00001588				777+X7	DS	OF	
00001588	E310 5014 0014		00000014	778+	LGF	R1, V1ADDR	load v1 source
0000158E	E751 0000 0806		00000000	779+	VL	v21, 0(R1)	use v21 to test decoder
00001594	E310 5018 0014		00000018	780+	LGF	R1, V2ADDR	load v2 source
0000159A	E761 0000 0806		00000000	781+	VL	v22, 0(R1)	use v22 to test decoder
000015A0	E310 501C 0014		0000001C	782+	LGF	R1, V3ADDR	load v3 source
000015A6	E771 0000 0806		00000000	783+	VL	v23, 0(R1)	use v23 to test decoder
000015AC	E756 7007 0E72			784+	VERIM	V21, V22, V23, 7, 0	test instruction
000015B2	E750 5030 080E		00001570	785+	VST	V21, V107	save v1 output
000015B8	07FB			786+	BR	R11	return
000015BC				787+RE7	DC	OF	xl16 expected result
000015BC				788+	DROP	R5	
000015BC	F0F0F1F1 F2F2F3F3			789	DC	XL16' F0F0F1F1F2F2F3F3 F4F4F5F5F6F6F7F7'	result t
000015C4	F4F4F5F5 F6F6F7F7						
000015CC	F0F0F0F0 F0F0F0F0			790	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
000015D4	F0F0F0F0 F0F0F0F0						
000015DC	00010203 04050607			791	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000015E4	08090A0B 0C0D0E0F						
000015EC	0F0F0F0F 0F0F0F0F			792	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000015F4	0F0F0F0F 0F0F0F0F						
				793			
00001600				794	VRI_D	VERIM, 255, 0	255->1 right
00001600		00001600		795+	DS	OFD	
00001600	00001648			796+	USING	*, R5	base for test data and test routine
00001604	0008			797+T8	DC	A(X8)	address of test routine
00001606	00			798+	DC	H' 8'	test number
00001606	00			799+	DC	X' 00'	
00001607	FF			800+	DC	HL1' 255'	i4 field
00001608	00			801+	DC	HL1' 0'	m5 field
00001609	E5C5D9C9 D4404040			802+	DC	CL8' VERIM	instruction name
00001614	0000168C			803+	DC	A(RE8+16)	address of v1 source
00001618	0000169C			804+	DC	A(RE8+32)	address of v2 source
0000161C	000016AC			805+	DC	A(RE8+48)	address of v3 source
00001620	00000010			806+	DC	A(16)	result length
00001624	0000167C			807+REA8	DC	A(RE8)	result address
00001628	00000000 00000000			808+	DS	FD	gap
00001630	00000000 00000000			809+V108	DS	XL16	V1 output
00001638	00000000 00000000						
00001640	00000000 00000000			810+	DS	FD	gap
				811+*			
00001648				812+X8	DS	OF	
00001648	E310 5014 0014		00000014	813+	LGF	R1, V1ADDR	load v1 source
0000164E	E751 0000 0806		00000000	814+	VL	v21, 0(R1)	use v21 to test decoder
00001654	E310 5018 0014		00000018	815+	LGF	R1, V2ADDR	load v2 source
0000165A	E761 0000 0806		00000000	816+	VL	v22, 0(R1)	use v22 to test decoder
00001660	E310 501C 0014		0000001C	817+	LGF	R1, V3ADDR	load v3 source
00001666	E771 0000 0806		00000000	818+	VL	v23, 0(R1)	use v23 to test decoder
0000166C	E756 70FF 0E72			819+	VERIM	V21, V22, V23, 255, 0	test instruction
00001672	E750 5030 080E		00001630	820+	VST	V21, V108	save v1 output
00001678	07FB			821+	BR	R11	return
0000167C				822+RE8	DC	OF	xl16 expected result
0000167C				823+	DROP	R5	
0000167C	F0F0F1F1 F2F2F3F3			824	DC	XL16' F0F0F1F1F2F2F3F3 F4F4F5F5F6F6F7F7'	result t
00001684	F4F4F5F5 F6F6F7F7						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000168C	F0F0F0F0 F0F0F0F0			825	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001694	F0F0F0F0 F0F0F0F0						
0000169C	00010203 04050607			826	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000016A4	08090A0B 0C0D0E0F						
000016AC	0F0F0F0F 0F0F0F0F			827	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000016B4	0F0F0F0F 0F0F0F0F						
				828			
				829	VRI_D	VERIM, 254, 0	254->2 right
000016C0				830+	DS	OFD	
000016C0		000016C0		831+	USING	*, R5	base for test data and test routine
000016C0	00001708			832+T9	DC	A(X9)	address of test routine
000016C4	0009			833+	DC	H' 9'	test number
000016C6	00			834+	DC	X' 00'	
000016C7	FE			835+	DC	HL1' 254'	i4 field
000016C8	00			836+	DC	HL1' 0'	m5 field
000016C9	E5C5D9C9 D4404040			837+	DC	CL8' VERIM	instruction name
000016D4	0000174C			838+	DC	A(RE9+16)	address of v1 source
000016D8	0000175C			839+	DC	A(RE9+32)	address of v2 source
000016DC	0000176C			840+	DC	A(RE9+48)	address of v3 source
000016E0	00000010			841+	DC	A(16)	result length
000016E4	0000173C			842+REA9	DC	A(RE9)	result address
000016E8	00000000 00000000			843+	DS	FD	gap
000016F0	00000000 00000000			844+V109	DS	XL16	V1 output
000016F8	00000000 00000000						
00001700	00000000 00000000			845+	DS	FD	gap
				846+*			
00001708				847+X9	DS	OF	
00001708	E310 5014 0014		00000014	848+	LGF	R1, V1ADDR	load v1 source
0000170E	E751 0000 0806		00000000	849+	VL	v21, 0(R1)	use v21 to test decoder
00001714	E310 5018 0014		00000018	850+	LGF	R1, V2ADDR	load v2 source
0000171A	E761 0000 0806		00000000	851+	VL	v22, 0(R1)	use v22 to test decoder
00001720	E310 501C 0014		0000001C	852+	LGF	R1, V3ADDR	load v3 source
00001726	E771 0000 0806		00000000	853+	VL	v23, 0(R1)	use v23 to test decoder
0000172C	E756 70FE 0E72			854+	VERIM	V21, V22, V23, 254, 0	test instruction
00001732	E750 5030 080E		000016F0	855+	VST	V21, V109	save v1 output
00001738	07FB			856+	BR	R11	return
0000173C				857+RE9	DC	OF	xl16 expected result
0000173C				858+	DROP	R5	
0000173C	F0F0F0F0 F1F1F1F1			859	DC	XL16' F0F0F0F0F1F1F1F1 F2F2F2F2F3F3F3F3'	result t
00001744	F2F2F2F2 F3F3F3F3						
0000174C	F0F0F0F0 F0F0F0F0			860	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001754	F0F0F0F0 F0F0F0F0						
0000175C	00010203 04050607			861	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001764	08090A0B 0C0D0E0F						
0000176C	0F0F0F0F 0F0F0F0F			862	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001774	0F0F0F0F 0F0F0F0F						
				863			
				864	VRI_D	VERIM, 250, 0	250->6 right
00001780				865+	DS	OFD	
00001780		00001780		866+	USING	*, R5	base for test data and test routine
00001780	000017C8			867+T10	DC	A(X10)	address of test routine
00001784	000A			868+	DC	H' 10'	test number
00001786	00			869+	DC	X' 00'	
00001787	FA			870+	DC	HL1' 250'	i4 field
00001788	00			871+	DC	HL1' 0'	m5 field
00001789	E5C5D9C9 D4404040			872+	DC	CL8' VERIM	instruction name

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001794	0000180C			873+	DC	A(RE10+16)	address of v1 source
00001798	0000181C			874+	DC	A(RE10+32)	address of v2 source
0000179C	0000182C			875+	DC	A(RE10+48)	address of v3 source
000017A0	00000010			876+	DC	A(16)	result length
000017A4	000017FC			877+REA10	DC	A(RE10)	result address
000017A8	00000000 00000000			878+	DS	FD	gap
000017B0	00000000 00000000			879+V1010	DS	XL16	V1 output
000017B8	00000000 00000000						
000017C0	00000000 00000000			880+	DS	FD	gap
				881+*			
000017C8				882+X10	DS	0F	
000017C8	E310 5014 0014		00000014	883+	LGF	R1, V1ADDR	load v1 source
000017CE	E751 0000 0806		00000000	884+	VL	v21, 0(R1)	use v21 to test decoder
000017D4	E310 5018 0014		00000018	885+	LGF	R1, V2ADDR	load v2 source
000017DA	E761 0000 0806		00000000	886+	VL	v22, 0(R1)	use v22 to test decoder
000017E0	E310 501C 0014		0000001C	887+	LGF	R1, V3ADDR	load v3 source
000017E6	E771 0000 0806		00000000	888+	VL	v23, 0(R1)	use v23 to test decoder
000017EC	E756 70FA 0E72			889+	VERIM	V21, V22, V23, 250, 0	test instruction
000017F2	E750 5030 080E		000017B0	890+	VST	V21, V1010	save v1 output
000017F8	07FB			891+	BR	R11	return
000017FC				892+RE10	DC	0F	xl16 expected result
000017FC				893+	DROP	R5	
000017FC	F0F4F8FC F0F4F8FC			894	DC	XL16' F0F4F8FCF0F4F8FC F0F4F8FCF0F4F8FC'	result t
00001804	F0F4F8FC F0F4F8FC						
0000180C	F0F0F0F0 F0F0F0F0			895	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001814	F0F0F0F0 F0F0F0F0						
0000181C	00010203 04050607			896	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001824	08090A0B 0C0D0E0F						
0000182C	0F0F0F0F 0F0F0F0F			897	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001834	0F0F0F0F 0F0F0F0F						
				898			
				899	VRI_D	VERIM, 248, 0	248-8 right
00001840				900+	DS	0FD	
00001840		00001840		901+	USING	*, R5	base for test data and test routine
00001840	00001888			902+T11	DC	A(X11)	address of test routine
00001844	000B			903+	DC	H' 11'	test number
00001846	00			904+	DC	X' 00'	
00001847	F8			905+	DC	HL1' 248'	i4 field
00001848	00			906+	DC	HL1' 0'	m5 field
00001849	E5C5D9C9 D4404040			907+	DC	CL8' VERIM	instruction name
00001854	000018CC			908+	DC	A(RE11+16)	address of v1 source
00001858	000018DC			909+	DC	A(RE11+32)	address of v2 source
0000185C	000018EC			910+	DC	A(RE11+48)	address of v3 source
00001860	00000010			911+	DC	A(16)	result length
00001864	000018BC			912+REA11	DC	A(RE11)	result address
00001868	00000000 00000000			913+	DS	FD	gap
00001870	00000000 00000000			914+V1011	DS	XL16	V1 output
00001878	00000000 00000000						
00001880	00000000 00000000			915+	DS	FD	gap
				916+*			
00001888				917+X11	DS	0F	
00001888	E310 5014 0014		00000014	918+	LGF	R1, V1ADDR	load v1 source
0000188E	E751 0000 0806		00000000	919+	VL	v21, 0(R1)	use v21 to test decoder
00001894	E310 5018 0014		00000018	920+	LGF	R1, V2ADDR	load v2 source
0000189A	E761 0000 0806		00000000	921+	VL	v22, 0(R1)	use v22 to test decoder
000018A0	E310 501C 0014		0000001C	922+	LGF	R1, V3ADDR	load v3 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				935 *Halfword		
				936	VRI_D VERIM, 0, 1	
00001900				937+	DS OFD	
00001900		00001900		938+	USING *, R5	base for test data and test routine
00001900	00001948			939+T12	DC A(X12)	address of test routine
00001904	000C			940+	DC H' 12'	test number
00001906	00			941+	DC X' 00'	
00001907	00			942+	DC HL1' 0'	i4 field
00001908	01			943+	DC HL1' 1'	m5 field
00001909	E5C5D9C9 D4404040			944+	DC CL8' VERIM	instruction name
00001914	0000198C			945+	DC A(RE12+16)	address of v1 source
00001918	0000199C			946+	DC A(RE12+32)	address of v2 source
0000191C	000019AC			947+	DC A(RE12+48)	address of v3 source
00001920	00000010			948+	DC A(16)	result length
00001924	0000197C			949+REA12	DC A(RE12)	result address
00001928	00000000 00000000			950+	DS FD	gap
00001930	00000000 00000000			951+V1012	DS XL16	V1 output
00001938	00000000 00000000					
00001940	00000000 00000000			952+	DS FD	gap
				953+*		
00001948				954+X12	DS OF	
00001948	E310 5014 0014		00000014	955+	LGF R1, V1ADDR	load v1 source
0000194E	E751 0000 0806		00000000	956+	VL v21, 0(R1)	use v21 to test decoder
00001954	E310 5018 0014		00000018	957+	LGF R1, V2ADDR	load v2 source
0000195A	E761 0000 0806		00000000	958+	VL v22, 0(R1)	use v22 to test decoder
00001960	E310 501C 0014		0000001C	959+	LGF R1, V3ADDR	load v3 source
00001966	E771 0000 0806		00000000	960+	VL v23, 0(R1)	use v23 to test decoder
0000196C	E756 7000 1E72			961+	VERIM V21, V22, V23, 0, 1	test instruction
00001972	E750 5030 080E		00001930	962+	VST V21, V1012	save v1 output
00001978	07FB			963+	BR R11	return
0000197C				964+RE12	DC OF	xl16 expected result
0000197C				965+	DROP R5	
0000197C	F0F1F2F3 F4F5F6F7			966	DC XL16' F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	result t
00001984	F8F9FAFB FCFDFEFF					
0000198C	F0F0F0F0 F0F0F0F0			967	DC XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001994	F0F0F0F0 F0F0F0F0					
0000199C	00010203 04050607			968	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000019A4	08090A0B 0C0D0E0F					
000019AC	0F0F0F0F 0F0F0F0F			969	DC XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000019B4	0F0F0F0F 0F0F0F0F					
				970		
				971	VRI_D VERIM, 1, 1	
000019C0				972+	DS OFD	
000019C0		000019C0		973+	USING *, R5	base for test data and test routine
000019C0	00001A08			974+T13	DC A(X13)	address of test routine
000019C4	000D			975+	DC H' 13'	test number
000019C6	00			976+	DC X' 00'	
000019C7	01			977+	DC HL1' 1'	i4 field
000019C8	01			978+	DC HL1' 1'	m5 field
000019C9	E5C5D9C9 D4404040			979+	DC CL8' VERIM	instruction name
000019D4	00001A4C			980+	DC A(RE13+16)	address of v1 source
000019D8	00001A5C			981+	DC A(RE13+32)	address of v2 source
000019DC	00001A6C			982+	DC A(RE13+48)	address of v3 source
000019E0	00000010			983+	DC A(16)	result length
000019E4	00001A3C			984+REA13	DC A(RE13)	result address
000019E8	00000000 00000000			985+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000019F0	00000000 00000000			986+V1013	DS	XL16	V1 output
000019F8	00000000 00000000						
00001A00	00000000 00000000			987+	DS	FD	gap
				988+*			
00001A08				989+X13	DS	0F	
00001A08	E310 5014 0014		00000014	990+	LGF	R1, V1ADDR	load v1 source
00001A0E	E751 0000 0806		00000000	991+	VL	v21, 0(R1)	use v21 to test decoder
00001A14	E310 5018 0014		00000018	992+	LGF	R1, V2ADDR	load v2 source
00001A1A	E761 0000 0806		00000000	993+	VL	v22, 0(R1)	use v22 to test decoder
00001A20	E310 501C 0014		0000001C	994+	LGF	R1, V3ADDR	load v3 source
00001A26	E771 0000 0806		00000000	995+	VL	v23, 0(R1)	use v23 to test decoder
00001A2C	E756 7001 1E72			996+	VERIM	V21, V22, V23, 1, 1	test instruction
00001A32	E750 5030 080E		000019F0	997+	VST	V21, V1013	save v1 output
00001A38	07FB			998+	BR	R11	return
00001A3C				999+RE13	DC	0F	xl16 expected result
00001A3C				1000+	DROP	R5	
00001A3C	F0F2F4F6 F8FAFCFE			1001	DC	XL16' F0F2F4F6F8FAFCFE F0F2F4F6F8FAFCFE'	result t
00001A44	F0F2F4F6 F8FAFCFE						
00001A4C	F0F0F0F0 F0F0F0F0			1002	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001A54	F0F0F0F0 F0F0F0F0						
00001A5C	00010203 04050607			1003	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001A64	08090A0B 0C0D0E0F						
00001A6C	0F0F0F0F 0F0F0F0F			1004	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001A74	0F0F0F0F 0F0F0F0F						
				1005			
				1006	VRI_D	VERIM, 2, 1	
00001A80				1007+	DS	0FD	
00001A80		00001A80		1008+	USING	*, R5	base for test data and test routine
00001A80	00001AC8			1009+T14	DC	A(X14)	address of test routine
00001A84	000E			1010+	DC	H' 14'	test number
00001A86	00			1011+	DC	X' 00'	
00001A87	02			1012+	DC	HL1' 2'	i4 field
00001A88	01			1013+	DC	HL1' 1'	m5 field
00001A89	E5C5D9C9 D4404040			1014+	DC	CL8' VERIM	instruction name
00001A94	00001B0C			1015+	DC	A(RE14+16)	address of v1 source
00001A98	00001B1C			1016+	DC	A(RE14+32)	address of v2 source
00001A9C	00001B2C			1017+	DC	A(RE14+48)	address of v3 source
00001AA0	00000010			1018+	DC	A(16)	result length
00001AA4	00001AFC			1019+REA14	DC	A(RE14)	result address
00001AA8	00000000 00000000			1020+	DS	FD	gap
00001AB0	00000000 00000000			1021+V1014	DS	XL16	V1 output
00001AB8	00000000 00000000						
00001AC0	00000000 00000000			1022+	DS	FD	gap
				1023+*			
00001AC8				1024+X14	DS	0F	
00001AC8	E310 5014 0014		00000014	1025+	LGF	R1, V1ADDR	load v1 source
00001ACE	E751 0000 0806		00000000	1026+	VL	v21, 0(R1)	use v21 to test decoder
00001AD4	E310 5018 0014		00000018	1027+	LGF	R1, V2ADDR	load v2 source
00001ADA	E761 0000 0806		00000000	1028+	VL	v22, 0(R1)	use v22 to test decoder
00001AE0	E310 501C 0014		0000001C	1029+	LGF	R1, V3ADDR	load v3 source
00001AE6	E771 0000 0806		00000000	1030+	VL	v23, 0(R1)	use v23 to test decoder
00001AEC	E756 7002 1E72			1031+	VERIM	V21, V22, V23, 2, 1	test instruction
00001AF2	E750 5030 080E		00001AB0	1032+	VST	V21, V1014	save v1 output
00001AF8	07FB			1033+	BR	R11	return
00001AFC				1034+RE14	DC	0F	xl16 expected result
00001AFC				1035+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001AFC	F0F4F8FC F0F4F8FC			1036	DC	XL16' F0F4F8FCF0F4F8FC F0F4F8FCF0F4F8FC'	result
00001B04	F0F4F8FC F0F4F8FC						
00001B0C	F0F0F0F0 F0F0F0F0			1037	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001B14	F0F0F0F0 F0F0F0F0						
00001B1C	00010203 04050607			1038	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001B24	08090A0B 0C0D0E0F						
00001B2C	0F0F0F0F 0F0F0F0F			1039	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001B34	0F0F0F0F 0F0F0F0F						
				1040			
00001B40				1041	VRI_D	VERIM, 5, 1	
				1042+	DS	0FD	
00001B40		00001B40		1043+	USING	*, R5	base for test data and test routine
00001B40	00001B88			1044+T15	DC	A(X15)	address of test routine
00001B44	000F			1045+	DC	H' 15'	test number
00001B46	00			1046+	DC	X' 00'	
00001B47	05			1047+	DC	HL1' 5'	i4 field
00001B48	01			1048+	DC	HL1' 1'	m5 field
00001B49	E5C5D9C9 D4404040			1049+	DC	CL8' VERIM	instruction name
00001B54	00001BCC			1050+	DC	A(RE15+16)	address of v1 source
00001B58	00001BDC			1051+	DC	A(RE15+32)	address of v2 source
00001B5C	00001BEC			1052+	DC	A(RE15+48)	address of v3 source
00001B60	00000010			1053+	DC	A(16)	result length
00001B64	00001BBC			1054+REA15	DC	A(RE15)	result address
00001B68	00000000 00000000			1055+	DS	FD	gap
00001B70	00000000 00000000			1056+V1015	DS	XL16	V1 output
00001B78	00000000 00000000						
00001B80	00000000 00000000			1057+	DS	FD	gap
				1058+*			
00001B88				1059+X15	DS	0F	
00001B88	E310 5014 0014		00000014	1060+	LGF	R1, V1ADDR	load v1 source
00001B8E	E751 0000 0806		00000000	1061+	VL	v21, 0(R1)	use v21 to test decoder
00001B94	E310 5018 0014		00000018	1062+	LGF	R1, V2ADDR	load v2 source
00001B9A	E761 0000 0806		00000000	1063+	VL	v22, 0(R1)	use v22 to test decoder
00001BA0	E310 501C 0014		0000001C	1064+	LGF	R1, V3ADDR	load v3 source
00001BA6	E771 0000 0806		00000000	1065+	VL	v23, 0(R1)	use v23 to test decoder
00001BAC	E756 7005 1E72			1066+	VERIM	V21, V22, V23, 5, 1	test instruction
00001BB2	E750 5030 080E		00001B70	1067+	VST	V21, V1015	save v1 output
00001BB8	07FB			1068+	BR	R11	return
00001BBC				1069+RE15	DC	0F	xl16 expected result
00001BBC				1070+	DROP	R5	
00001BBC	F0F0F0F0 F0F0F0F0			1071	DC	XL16' F0F0F0F0F0F0F0F0 F1F1F1F1F1F1F1F1'	result
00001BC4	F1F1F1F1 F1F1F1F1						
00001BCC	F0F0F0F0 F0F0F0F0			1072	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001BD4	F0F0F0F0 F0F0F0F0						
00001BDC	00010203 04050607			1073	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001BE4	08090A0B 0C0D0E0F						
00001BEC	0F0F0F0F 0F0F0F0F			1074	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001BF4	0F0F0F0F 0F0F0F0F						
				1075			
00001C00				1076	VRI_D	VERIM, 7, 1	
				1077+	DS	0FD	
00001C00		00001C00		1078+	USING	*, R5	base for test data and test routine
00001C00	00001C48			1079+T16	DC	A(X16)	address of test routine
00001C04	0010			1080+	DC	H' 16'	test number
00001C06	00			1081+	DC	X' 00'	
00001C07	07			1082+	DC	HL1' 7'	i4 field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001C08	01			1083+	DC	HL1' 1'	m5 field
00001C09	E5C5D9C9 D4404040			1084+	DC	CL8' VERIM	instruction name
00001C14	00001C8C			1085+	DC	A(RE16+16)	address of v1 source
00001C18	00001C9C			1086+	DC	A(RE16+32)	address of v2 source
00001C1C	00001CAC			1087+	DC	A(RE16+48)	address of v3 source
00001C20	00000010			1088+	DC	A(16)	result length
00001C24	00001C7C			1089+REA16	DC	A(RE16)	result address
00001C28	00000000 00000000			1090+	DS	FD	gap
00001C30	00000000 00000000			1091+V1016	DS	XL16	V1 output
00001C38	00000000 00000000						
00001C40	00000000 00000000			1092+	DS	FD	gap
				1093+*			
00001C48				1094+X16	DS	0F	
00001C48	E310 5014 0014		00000014	1095+	LGF	R1, V1ADDR	load v1 source
00001C4E	E751 0000 0806		00000000	1096+	VL	v21, 0(R1)	use v21 to test decoder
00001C54	E310 5018 0014		00000018	1097+	LGF	R1, V2ADDR	load v2 source
00001C5A	E761 0000 0806		00000000	1098+	VL	v22, 0(R1)	use v22 to test decoder
00001C60	E310 501C 0014		0000001C	1099+	LGF	R1, V3ADDR	load v3 source
00001C66	E771 0000 0806		00000000	1100+	VL	v23, 0(R1)	use v23 to test decoder
00001C6C	E756 7007 1E72			1101+	VERIM	V21, V22, V23, 7, 1	test instruction
00001C72	E750 5030 080E		00001C30	1102+	VST	V21, V1016	save v1 output
00001C78	07FB			1103+	BR	R11	return
00001C7C				1104+RE16	DC	0F	xl16 expected result
00001C7C				1105+	DROP	R5	
00001C7C	F0F0F1F1 F2F2F3F3			1106	DC	XL16' F0F0F1F1F2F2F3F3 F4F4F5F5F6F6F7F7'	result t
00001C84	F4F4F5F5 F6F6F7F7						
00001C8C	F0F0F0F0 F0F0F0F0			1107	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001C94	F0F0F0F0 F0F0F0F0						
00001C9C	00010203 04050607			1108	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001CA4	08090A0B 0C0D0E0F						
00001CAC	0F0F0F0F 0F0F0F0F			1109	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001CB4	0F0F0F0F 0F0F0F0F						
				1110			
				1111	VRI_D	VERIM, 255, 1	255->1 right
00001CC0				1112+	DS	0FD	
00001CC0		00001CC0		1113+	USING	*, R5	base for test data and test routine
00001CC0	00001D08			1114+T17	DC	A(X17)	address of test routine
00001CC4	0011			1115+	DC	H' 17'	test number
00001CC6	00			1116+	DC	X' 00'	
00001CC7	FF			1117+	DC	HL1' 255'	i4 field
00001CC8	01			1118+	DC	HL1' 1'	m5 field
00001CC9	E5C5D9C9 D4404040			1119+	DC	CL8' VERIM	instruction name
00001CD4	00001D4C			1120+	DC	A(RE17+16)	address of v1 source
00001CD8	00001D5C			1121+	DC	A(RE17+32)	address of v2 source
00001CDC	00001D6C			1122+	DC	A(RE17+48)	address of v3 source
00001CE0	00000010			1123+	DC	A(16)	result length
00001CE4	00001D3C			1124+REA17	DC	A(RE17)	result address
00001CE8	00000000 00000000			1125+	DS	FD	gap
00001CF0	00000000 00000000			1126+V1017	DS	XL16	V1 output
00001CF8	00000000 00000000						
00001D00	00000000 00000000			1127+	DS	FD	gap
				1128+*			
00001D08				1129+X17	DS	0F	
00001D08	E310 5014 0014		00000014	1130+	LGF	R1, V1ADDR	load v1 source
00001D0E	E751 0000 0806		00000000	1131+	VL	v21, 0(R1)	use v21 to test decoder
00001D14	E310 5018 0014		00000018	1132+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00001D1A	E761 0000 0806		00000000	1133+	VL	v22, 0(R1)	use v22 to test decoder
00001D20	E310 501C 0014		0000001C	1134+	LGF	R1, V3ADDR	load v3 source
00001D26	E771 0000 0806		00000000	1135+	VL	v23, 0(R1)	use v23 to test decoder
00001D2C	E756 70FF 1E72			1136+	VERIM	V21, V22, V23, 255, 1	test instruction
00001D32	E750 5030 080E		00001CF0	1137+	VST	V21, V1017	save v1 output
00001D38	07FB			1138+	BR	R11	return
00001D3C				1139+RE17	DC	0F	xl16 expected result
00001D3C				1140+	DROP	R5	
00001D3C	F0F0F1F1 F2F2F3F3			1141	DC	XL16' F0F0F1F1F2F2F3F3 F4F4F5F5F6F6F7F7'	result t
00001D44	F4F4F5F5 F6F6F7F7						
00001D4C	F0F0F0F0 F0F0F0F0			1142	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001D54	F0F0F0F0 F0F0F0F0						
00001D5C	00010203 04050607			1143	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001D64	08090A0B 0C0D0E0F						
00001D6C	0F0F0F0F 0F0F0F0F			1144	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001D74	0F0F0F0F 0F0F0F0F						
				1145			
00001D80				1146	VRI_D	VERIM, 254, 1	254->2 right
00001D80		00001D80		1147+	DS	0FD	
00001D80	00001DC8			1148+	USING	*, R5	base for test data and test routine
00001D84	0012			1149+T18	DC	A(X18)	address of test routine
00001D86	00			1150+	DC	H' 18'	test number
00001D87	FE			1151+	DC	X' 00'	
00001D88	01			1152+	DC	HL1' 254'	i4 field
00001D89	E5C5D9C9 D4404040			1153+	DC	HL1' 1'	m5 field
00001D94	00001E0C			1154+	DC	CL8' VERIM	instruction name
00001D98	00001E1C			1155+	DC	A(RE18+16)	address of v1 source
00001D9C	00001E2C			1156+	DC	A(RE18+32)	address of v2 source
00001DA0	00000010			1157+	DC	A(RE18+48)	address of v3 source
00001DA4	00001DFC			1158+	DC	A(16)	result length
00001DA8	00000000 00000000			1159+REA18	DC	A(RE18)	result address
00001DB0	00000000 00000000			1160+	DS	FD	gap
00001DB8	00000000 00000000			1161+V1018	DS	XL16	V1 output
00001DC0	00000000 00000000			1162+	DS	FD	gap
				1163+*			
00001DC8				1164+X18	DS	0F	
00001DC8	E310 5014 0014		00000014	1165+	LGF	R1, V1ADDR	load v1 source
00001DCE	E751 0000 0806		00000000	1166+	VL	v21, 0(R1)	use v21 to test decoder
00001DD4	E310 5018 0014		00000018	1167+	LGF	R1, V2ADDR	load v2 source
00001DDA	E761 0000 0806		00000000	1168+	VL	v22, 0(R1)	use v22 to test decoder
00001DE0	E310 501C 0014		0000001C	1169+	LGF	R1, V3ADDR	load v3 source
00001DE6	E771 0000 0806		00000000	1170+	VL	v23, 0(R1)	use v23 to test decoder
00001DEC	E756 70FE 1E72			1171+	VERIM	V21, V22, V23, 254, 1	test instruction
00001DF2	E750 5030 080E		00001DB0	1172+	VST	V21, V1018	save v1 output
00001DF8	07FB			1173+	BR	R11	return
00001DFC				1174+RE18	DC	0F	xl16 expected result
00001DFC				1175+	DROP	R5	
00001DFC	F0F0F0F0 F1F1F1F1			1176	DC	XL16' F0F0F0F0F1F1F1F1 F2F2F2F2F3F3F3F3'	result t
00001E04	F2F2F2F2 F3F3F3F3						
00001E0C	F0F0F0F0 F0F0F0F0			1177	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001E14	F0F0F0F0 F0F0F0F0						
00001E1C	00010203 04050607			1178	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001E24	08090A0B 0C0D0E0F						
00001E2C	0F0F0F0F 0F0F0F0F			1179	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001E34	0F0F0F0F 0F0F0F0F						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1180		
				1181	VRI_D VERIM, 250, 1	250->6 right
00001E40				1182+	DS OFD	
00001E40		00001E40		1183+	USING *, R5	base for test data and test routine
00001E40	00001E88			1184+T19	DC A(X19)	address of test routine
00001E44	0013			1185+	DC H' 19'	test number
00001E46	00			1186+	DC X' 00'	
00001E47	FA			1187+	DC HL1' 250'	i4 field
00001E48	01			1188+	DC HL1' 1'	m5 field
00001E49	E5C5D9C9 D4404040			1189+	DC CL8' VERIM	instruction name
00001E54	00001ECC			1190+	DC A(RE19+16)	address of v1 source
00001E58	00001EDC			1191+	DC A(RE19+32)	address of v2 source
00001E5C	00001EEC			1192+	DC A(RE19+48)	address of v3 source
00001E60	00000010			1193+	DC A(16)	result length
00001E64	00001EBC			1194+REA19	DC A(RE19)	result address
00001E68	00000000 00000000			1195+	DS FD	gap
00001E70	00000000 00000000			1196+V1019	DS XL16	V1 output
00001E78	00000000 00000000					
00001E80	00000000 00000000			1197+	DS FD	gap
				1198+*		
00001E88				1199+X19	DS OF	
00001E88	E310 5014 0014		00000014	1200+	LGF R1, V1ADDR	load v1 source
00001E8E	E751 0000 0806		00000000	1201+	VL v21, 0(R1)	use v21 to test decoder
00001E94	E310 5018 0014		00000018	1202+	LGF R1, V2ADDR	load v2 source
00001E9A	E761 0000 0806		00000000	1203+	VL v22, 0(R1)	use v22 to test decoder
00001EA0	E310 501C 0014		0000001C	1204+	LGF R1, V3ADDR	load v3 source
00001EA6	E771 0000 0806		00000000	1205+	VL v23, 0(R1)	use v23 to test decoder
00001EAC	E756 70FA 1E72			1206+	VERIM V21, V22, V23, 250, 1	test instruction
00001EB2	E750 5030 080E		00001E70	1207+	VST V21, V1019	save v1 output
00001EB8	07FB			1208+	BR R11	return
00001EBC				1209+RE19	DC OF	xl16 expected result
00001EBC				1210+	DROP R5	
00001EBC	F4F0FCF8 F4F0FCF8			1211	DC XL16' F4F0FCF8F4F0FCF8 F4F0FCF8F4F0FCF8'	result t
00001EC4	F4F0FCF8 F4F0FCF8					
00001ECC	F0F0F0F0 F0F0F0F0			1212	DC XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00001ED4	F0F0F0F0 F0F0F0F0					
00001EDC	00010203 04050607			1213	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00001EE4	08090A0B 0C0D0E0F					
00001EEC	0F0F0F0F 0F0F0F0F			1214	DC XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00001EF4	0F0F0F0F 0F0F0F0F					
				1215		
				1216	VRI_D VERIM, 248, 1	248-8 right
00001F00				1217+	DS OFD	
00001F00		00001F00		1218+	USING *, R5	base for test data and test routine
00001F00	00001F48			1219+T20	DC A(X20)	address of test routine
00001F04	0014			1220+	DC H' 20'	test number
00001F06	00			1221+	DC X' 00'	
00001F07	F8			1222+	DC HL1' 248'	i4 field
00001F08	01			1223+	DC HL1' 1'	m5 field
00001F09	E5C5D9C9 D4404040			1224+	DC CL8' VERIM	instruction name
00001F14	00001F8C			1225+	DC A(RE20+16)	address of v1 source
00001F18	00001F9C			1226+	DC A(RE20+32)	address of v2 source
00001F1C	00001FAC			1227+	DC A(RE20+48)	address of v3 source
00001F20	00000010			1228+	DC A(16)	result length
00001F24	00001F7C			1229+REA20	DC A(RE20)	result address
00001F28	00000000 00000000			1230+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1251 *Word		
				1252	VRI_D VERIM, 0, 2	
00001FC0				1253+	DS OFD	
00001FC0		00001FC0		1254+	USING *, R5	base for test data and test routine
00001FC0	00002008			1255+T21	DC A(X21)	address of test routine
00001FC4	0015			1256+	DC H' 21'	test number
00001FC6	00			1257+	DC X' 00'	
00001FC7	00			1258+	DC HL1' 0'	i4 field
00001FC8	02			1259+	DC HL1' 2'	m5 field
00001FC9	E5C5D9C9 D4404040			1260+	DC CL8' VERIM	instruction name
00001FD4	0000204C			1261+	DC A(RE21+16)	address of v1 source
00001FD8	0000205C			1262+	DC A(RE21+32)	address of v2 source
00001FDC	0000206C			1263+	DC A(RE21+48)	address of v3 source
00001FE0	00000010			1264+	DC A(16)	result length
00001FE4	0000203C			1265+REA21	DC A(RE21)	result address
00001FE8	00000000 00000000			1266+	DS FD	gap
00001FF0	00000000 00000000			1267+V1021	DS XL16	V1 output
00001FF8	00000000 00000000					
00002000	00000000 00000000			1268+	DS FD	gap
				1269+*		
00002008				1270+X21	DS OF	
00002008	E310 5014 0014		00000014	1271+	LGF R1, V1ADDR	load v1 source
0000200E	E751 0000 0806		00000000	1272+	VL v21, 0(R1)	use v21 to test decoder
00002014	E310 5018 0014		00000018	1273+	LGF R1, V2ADDR	load v2 source
0000201A	E761 0000 0806		00000000	1274+	VL v22, 0(R1)	use v22 to test decoder
00002020	E310 501C 0014		0000001C	1275+	LGF R1, V3ADDR	load v3 source
00002026	E771 0000 0806		00000000	1276+	VL v23, 0(R1)	use v23 to test decoder
0000202C	E756 7000 2E72			1277+	VERIM V21, V22, V23, 0, 2	test instruction
00002032	E750 5030 080E		00001FF0	1278+	VST V21, V1021	save v1 output
00002038	07FB			1279+	BR R11	return
0000203C				1280+RE21	DC OF	xl16 expected result
0000203C				1281+	DROP R5	
0000203C	F0F1F2F3 F4F5F6F7			1282	DC XL16' F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	result t
00002044	F8F9FAFB FCFDFEFF					
0000204C	F0F0F0F0 F0F0F0F0			1283	DC XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002054	F0F0F0F0 F0F0F0F0					
0000205C	00010203 04050607			1284	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002064	08090A0B 0C0D0E0F					
0000206C	0F0F0F0F 0F0F0F0F			1285	DC XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002074	0F0F0F0F 0F0F0F0F					
				1286		
				1287	VRI_D VERIM, 1, 2	
00002080				1288+	DS OFD	
00002080		00002080		1289+	USING *, R5	base for test data and test routine
00002080	000020C8			1290+T22	DC A(X22)	address of test routine
00002084	0016			1291+	DC H' 22'	test number
00002086	00			1292+	DC X' 00'	
00002087	01			1293+	DC HL1' 1'	i4 field
00002088	02			1294+	DC HL1' 2'	m5 field
00002089	E5C5D9C9 D4404040			1295+	DC CL8' VERIM	instruction name
00002094	0000210C			1296+	DC A(RE22+16)	address of v1 source
00002098	0000211C			1297+	DC A(RE22+32)	address of v2 source
0000209C	0000212C			1298+	DC A(RE22+48)	address of v3 source
000020A0	00000010			1299+	DC A(16)	result length
000020A4	000020FC			1300+REA22	DC A(RE22)	result address
000020A8	00000000 00000000			1301+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000020B0	00000000 00000000			1302+V1022	DS	XL16	V1 output
000020B8	00000000 00000000						
000020C0	00000000 00000000			1303+	DS	FD	gap
				1304+*			
000020C8				1305+X22	DS	0F	
000020C8	E310 5014 0014		00000014	1306+	LGF	R1, V1ADDR	load v1 source
000020CE	E751 0000 0806		00000000	1307+	VL	v21, 0(R1)	use v21 to test decoder
000020D4	E310 5018 0014		00000018	1308+	LGF	R1, V2ADDR	load v2 source
000020DA	E761 0000 0806		00000000	1309+	VL	v22, 0(R1)	use v22 to test decoder
000020E0	E310 501C 0014		0000001C	1310+	LGF	R1, V3ADDR	load v3 source
000020E6	E771 0000 0806		00000000	1311+	VL	v23, 0(R1)	use v23 to test decoder
000020EC	E756 7001 2E72			1312+	VERIM	V21, V22, V23, 1, 2	test instruction
000020F2	E750 5030 080E		000020B0	1313+	VST	V21, V1022	save v1 output
000020F8	07FB			1314+	BR	R11	return
000020FC				1315+RE22	DC	0F	xl16 expected result
000020FC				1316+	DROP	R5	
000020FC	F0F2F4F6 F8FAFCFE			1317	DC	XL16' F0F2F4F6F8FAFCFE F0F2F4F6F8FAFCFE'	result t
00002104	F0F2F4F6 F8FAFCFE						
0000210C	F0F0F0F0 F0F0F0F0			1318	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002114	F0F0F0F0 F0F0F0F0						
0000211C	00010203 04050607			1319	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002124	08090A0B 0C0D0E0F						
0000212C	0F0F0F0F 0F0F0F0F			1320	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002134	0F0F0F0F 0F0F0F0F						
				1321			
				1322	VRI_D	VERIM, 2, 2	
00002140				1323+	DS	0FD	
00002140		00002140		1324+	USING	*, R5	base for test data and test routine
00002140	00002188			1325+T23	DC	A(X23)	address of test routine
00002144	0017			1326+	DC	H' 23'	test number
00002146	00			1327+	DC	X' 00'	
00002147	02			1328+	DC	HL1' 2'	i4 field
00002148	02			1329+	DC	HL1' 2'	m5 field
00002149	E5C5D9C9 D4404040			1330+	DC	CL8' VERIM	instruction name
00002154	000021CC			1331+	DC	A(RE23+16)	address of v1 source
00002158	000021DC			1332+	DC	A(RE23+32)	address of v2 source
0000215C	000021EC			1333+	DC	A(RE23+48)	address of v3 source
00002160	00000010			1334+	DC	A(16)	result length
00002164	000021BC			1335+REA23	DC	A(RE23)	result address
00002168	00000000 00000000			1336+	DS	FD	gap
00002170	00000000 00000000			1337+V1023	DS	XL16	V1 output
00002178	00000000 00000000						
00002180	00000000 00000000			1338+	DS	FD	gap
				1339+*			
00002188				1340+X23	DS	0F	
00002188	E310 5014 0014		00000014	1341+	LGF	R1, V1ADDR	load v1 source
0000218E	E751 0000 0806		00000000	1342+	VL	v21, 0(R1)	use v21 to test decoder
00002194	E310 5018 0014		00000018	1343+	LGF	R1, V2ADDR	load v2 source
0000219A	E761 0000 0806		00000000	1344+	VL	v22, 0(R1)	use v22 to test decoder
000021A0	E310 501C 0014		0000001C	1345+	LGF	R1, V3ADDR	load v3 source
000021A6	E771 0000 0806		00000000	1346+	VL	v23, 0(R1)	use v23 to test decoder
000021AC	E756 7002 2E72			1347+	VERIM	V21, V22, V23, 2, 2	test instruction
000021B2	E750 5030 080E		00002170	1348+	VST	V21, V1023	save v1 output
000021B8	07FB			1349+	BR	R11	return
000021BC				1350+RE23	DC	0F	xl16 expected result
000021BC				1351+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000021BC	F0F4F8FC F0F4F8FC			1352	DC	XL16' F0F4F8FCF0F4F8FC F0F4F8FCF0F4F8FC'	result
000021C4	F0F4F8FC F0F4F8FC						
000021CC	F0F0F0F0 F0F0F0F0			1353	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
000021D4	F0F0F0F0 F0F0F0F0						
000021DC	00010203 04050607			1354	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000021E4	08090A0B 0C0D0E0F						
000021EC	0F0F0F0F 0F0F0F0F			1355	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000021F4	0F0F0F0F 0F0F0F0F						
				1356			
				1357	VRI_D	VERIM, 5, 2	
00002200				1358+	DS	OFD	
00002200		00002200		1359+	USING	*, R5	base for test data and test routine
00002200	00002248			1360+T24	DC	A(X24)	address of test routine
00002204	0018			1361+	DC	H' 24'	test number
00002206	00			1362+	DC	X' 00'	
00002207	05			1363+	DC	HL1' 5'	i4 field
00002208	02			1364+	DC	HL1' 2'	m5 field
00002209	E5C5D9C9 D4404040			1365+	DC	CL8' VERIM	instruction name
00002214	0000228C			1366+	DC	A(RE24+16)	address of v1 source
00002218	0000229C			1367+	DC	A(RE24+32)	address of v2 source
0000221C	000022AC			1368+	DC	A(RE24+48)	address of v3 source
00002220	00000010			1369+	DC	A(16)	result length
00002224	0000227C			1370+REA24	DC	A(RE24)	result address
00002228	00000000 00000000			1371+	DS	FD	gap
00002230	00000000 00000000			1372+V1024	DS	XL16	V1 output
00002238	00000000 00000000						
00002240	00000000 00000000			1373+	DS	FD	gap
				1374+*			
00002248				1375+X24	DS	OF	
00002248	E310 5014 0014		00000014	1376+	LGF	R1, V1ADDR	load v1 source
0000224E	E751 0000 0806		00000000	1377+	VL	v21, 0(R1)	use v21 to test decoder
00002254	E310 5018 0014		00000018	1378+	LGF	R1, V2ADDR	load v2 source
0000225A	E761 0000 0806		00000000	1379+	VL	v22, 0(R1)	use v22 to test decoder
00002260	E310 501C 0014		0000001C	1380+	LGF	R1, V3ADDR	load v3 source
00002266	E771 0000 0806		00000000	1381+	VL	v23, 0(R1)	use v23 to test decoder
0000226C	E756 7005 2E72			1382+	VERIM	V21, V22, V23, 5, 2	test instruction
00002272	E750 A030 080E		00002230	1383+	VST	V21, V1024	save v1 output
00002278	07FB			1384+	BR	R11	return
0000227C				1385+RE24	DC	OF	xl16 expected result
0000227C				1386+	DROP	R5	
0000227C	F0F0F0F0 F0F0F0F0			1387	DC	XL16' F0F0F0F0F0F0F0F0 F1F1F1F1F1F1F1F1'	result
00002284	F1F1F1F1 F1F1F1F1						
0000228C	F0F0F0F0 F0F0F0F0			1388	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002294	F0F0F0F0 F0F0F0F0						
0000229C	00010203 04050607			1389	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000022A4	08090A0B 0C0D0E0F						
000022AC	0F0F0F0F 0F0F0F0F			1390	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000022B4	0F0F0F0F 0F0F0F0F						
				1391			
				1392	VRI_D	VERIM, 7, 2	
000022C0				1393+	DS	OFD	
000022C0		000022C0		1394+	USING	*, R5	base for test data and test routine
000022C0	00002308			1395+T25	DC	A(X25)	address of test routine
000022C4	0019			1396+	DC	H' 25'	test number
000022C6	00			1397+	DC	X' 00'	
000022C7	07			1398+	DC	HL1' 7'	i4 field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000022C8	02			1399+	DC	HL1' 2'	m5 field
000022C9	E5C5D9C9 D4404040			1400+	DC	CL8' VERIM	instruction name
000022D4	0000234C			1401+	DC	A(RE25+16)	address of v1 source
000022D8	0000235C			1402+	DC	A(RE25+32)	address of v2 source
000022DC	0000236C			1403+	DC	A(RE25+48)	address of v3 source
000022E0	00000010			1404+	DC	A(16)	result length
000022E4	0000233C			1405+REA25	DC	A(RE25)	result address
000022E8	00000000 00000000			1406+	DS	FD	gap
000022F0	00000000 00000000			1407+V1025	DS	XL16	V1 output
000022F8	00000000 00000000						
00002300	00000000 00000000			1408+	DS	FD	gap
				1409+*			
00002308				1410+X25	DS	0F	
00002308	E310 5014 0014		00000014	1411+	LGF	R1, V1ADDR	load v1 source
0000230E	E751 0000 0806		00000000	1412+	VL	v21, 0(R1)	use v21 to test decoder
00002314	E310 5018 0014		00000018	1413+	LGF	R1, V2ADDR	load v2 source
0000231A	E761 0000 0806		00000000	1414+	VL	v22, 0(R1)	use v22 to test decoder
00002320	E310 501C 0014		0000001C	1415+	LGF	R1, V3ADDR	load v3 source
00002326	E771 0000 0806		00000000	1416+	VL	v23, 0(R1)	use v23 to test decoder
0000232C	E756 7007 2E72			1417+	VERIM	V21, V22, V23, 7, 2	test instruction
00002332	E750 5030 080E		000022F0	1418+	VST	V21, V1025	save v1 output
00002338	07FB			1419+	BR	R11	return
0000233C				1420+RE25	DC	0F	xl16 expected result
0000233C				1421+	DROP	R5	
0000233C	F0F1F1F0 F2F3F3F2			1422	DC	XL16' F0F1F1F0F2F3F3F2 F4F5F5F4F6F7F7F6'	result t
00002344	F4F5F5F4 F6F7F7F6						
0000234C	F0F0F0F0 F0F0F0F0			1423	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002354	F0F0F0F0 F0F0F0F0						
0000235C	00010203 04050607			1424	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002364	08090A0B 0C0D0E0F						
0000236C	0F0F0F0F 0F0F0F0F			1425	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002374	0F0F0F0F 0F0F0F0F						
				1426			
				1427	VRI_D	VERIM, 255, 2	255->1 right
00002380				1428+	DS	0FD	
00002380		00002380		1429+	USING	*, R5	base for test data and test routine
00002380	000023C8			1430+T26	DC	A(X26)	address of test routine
00002384	001A			1431+	DC	H' 26'	test number
00002386	00			1432+	DC	X' 00'	
00002387	FF			1433+	DC	HL1' 255'	i4 field
00002388	02			1434+	DC	HL1' 2'	m5 field
00002389	E5C5D9C9 D4404040			1435+	DC	CL8' VERIM	instruction name
00002394	0000240C			1436+	DC	A(RE26+16)	address of v1 source
00002398	0000241C			1437+	DC	A(RE26+32)	address of v2 source
0000239C	0000242C			1438+	DC	A(RE26+48)	address of v3 source
000023A0	00000010			1439+	DC	A(16)	result length
000023A4	000023FC			1440+REA26	DC	A(RE26)	result address
000023A8	00000000 00000000			1441+	DS	FD	gap
000023B0	00000000 00000000			1442+V1026	DS	XL16	V1 output
000023B8	00000000 00000000						
000023C0	00000000 00000000			1443+	DS	FD	gap
				1444+*			
000023C8				1445+X26	DS	0F	
000023C8	E310 5014 0014		00000014	1446+	LGF	R1, V1ADDR	load v1 source
000023CE	E751 0000 0806		00000000	1447+	VL	v21, 0(R1)	use v21 to test decoder
000023D4	E310 5018 0014		00000018	1448+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000023DA	E761 0000 0806		00000000	1449+	VL	v22, 0(R1)	use v22 to test decoder
000023E0	E310 501C 0014		0000001C	1450+	LGF	R1, V3ADDR	load v3 source
000023E6	E771 0000 0806		00000000	1451+	VL	v23, 0(R1)	use v23 to test decoder
000023EC	E756 70FF 2E72			1452+	VERIM	V21, V22, V23, 255, 2	test instruction
000023F2	E750 5030 080E		000023B0	1453+	VST	V21, V1026	save v1 output
000023F8	07FB			1454+	BR	R11	return
000023FC				1455+RE26	DC	0F	xl16 expected result
000023FC				1456+	DROP	R5	
000023FC	F0F0F1F1 F2F2F3F3			1457	DC	XL16' F0F0F1F1F2F2F3F3 F4F4F5F5F6F6F7F7'	result t
00002404	F4F4F5F5 F6F6F7F7						
0000240C	F0F0F0F0 F0F0F0F0			1458	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002414	F0F0F0F0 F0F0F0F0						
0000241C	00010203 04050607			1459	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002424	08090A0B 0C0D0E0F						
0000242C	0F0F0F0F 0F0F0F0F			1460	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002434	0F0F0F0F 0F0F0F0F						
				1461			
00002440				1462	VRI_D	VERIM, 254, 2	254->2 right
00002440		00002440		1463+	DS	0FD	
00002440	00002488			1464+	USING	*, R5	base for test data and test routine
00002444	001B			1465+T27	DC	A(X27)	address of test routine
00002446	00			1466+	DC	H' 27'	test number
00002447	FE			1467+	DC	X' 00'	
00002448	02			1468+	DC	HL1' 254'	i4 field
00002449	E5C5D9C9 D4404040			1469+	DC	HL1' 2'	m5 field
00002454	000024CC			1470+	DC	CL8' VERIM	instruction name
00002458	000024DC			1471+	DC	A(RE27+16)	address of v1 source
0000245C	000024EC			1472+	DC	A(RE27+32)	address of v2 source
00002460	00000010			1473+	DC	A(RE27+48)	address of v3 source
00002464	000024BC			1474+	DC	A(16)	result length
00002468	00000000 00000000			1475+REA27	DC	A(RE27)	result address
00002470	00000000 00000000			1476+	DS	FD	gap
00002478	00000000 00000000			1477+V1027	DS	XL16	V1 output
00002480	00000000 00000000			1478+	DS	FD	gap
				1479+*			
00002488				1480+X27	DS	0F	
00002488	E310 5014 0014		00000014	1481+	LGF	R1, V1ADDR	load v1 source
0000248E	E751 0000 0806		00000000	1482+	VL	v21, 0(R1)	use v21 to test decoder
00002494	E310 5018 0014		00000018	1483+	LGF	R1, V2ADDR	load v2 source
0000249A	E761 0000 0806		00000000	1484+	VL	v22, 0(R1)	use v22 to test decoder
000024A0	E310 501C 0014		0000001C	1485+	LGF	R1, V3ADDR	load v3 source
000024A6	E771 0000 0806		00000000	1486+	VL	v23, 0(R1)	use v23 to test decoder
000024AC	E756 70FE 2E72			1487+	VERIM	V21, V22, V23, 254, 2	test instruction
000024B2	E750 5030 080E		00002470	1488+	VST	V21, V1027	save v1 output
000024B8	07FB			1489+	BR	R11	return
000024BC				1490+RE27	DC	0F	xl16 expected result
000024BC				1491+	DROP	R5	
000024BC	F0F0F0F0 F1F1F1F1			1492	DC	XL16' F0F0F0F0F1F1F1F1 F2F2F2F2F3F3F3F3'	result t
000024C4	F2F2F2F2 F3F3F3F3						
000024CC	F0F0F0F0 F0F0F0F0			1493	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
000024D4	F0F0F0F0 F0F0F0F0						
000024DC	00010203 04050607			1494	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000024E4	08090A0B 0C0D0E0F						
000024EC	0F0F0F0F 0F0F0F0F			1495	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000024F4	0F0F0F0F 0F0F0F0F						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1496		
				1497	VRI_D VERIM, 250, 2	250->6 right
00002500				1498+	DS OFD	
00002500		00002500		1499+	USING *, R5	base for test data and test routine
00002500	00002548			1500+T28	DC A(X28)	address of test routine
00002504	001C			1501+	DC H' 28'	test number
00002506	00			1502+	DC X' 00'	
00002507	FA			1503+	DC HL1' 250'	i4 field
00002508	02			1504+	DC HL1' 2'	m5 field
00002509	E5C5D9C9 D4404040			1505+	DC CL8' VERIM	instruction name
00002514	0000258C			1506+	DC A(RE28+16)	address of v1 source
00002518	0000259C			1507+	DC A(RE28+32)	address of v2 source
0000251C	000025AC			1508+	DC A(RE28+48)	address of v3 source
00002520	00000010			1509+	DC A(16)	result length
00002524	0000257C			1510+REA28	DC A(RE28)	result address
00002528	00000000 00000000			1511+	DS FD	gap
00002530	00000000 00000000			1512+V1028	DS XL16	V1 output
00002538	00000000 00000000					
00002540	00000000 00000000			1513+	DS FD	gap
				1514+*		
00002548				1515+X28	DS OF	
00002548	E310 5014 0014		00000014	1516+	LGF R1, V1ADDR	load v1 source
0000254E	E751 0000 0806		00000000	1517+	VL v21, 0(R1)	use v21 to test decoder
00002554	E310 5018 0014		00000018	1518+	LGF R1, V2ADDR	load v2 source
0000255A	E761 0000 0806		00000000	1519+	VL v22, 0(R1)	use v22 to test decoder
00002560	E310 501C 0014		0000001C	1520+	LGF R1, V3ADDR	load v3 source
00002566	E771 0000 0806		00000000	1521+	VL v23, 0(R1)	use v23 to test decoder
0000256C	E756 70FA 2E72			1522+	VERIM V21, V22, V23, 250, 2	test instruction
00002572	E750 5030 080E		00002530	1523+	VST V21, V1028	save v1 output
00002578	07FB			1524+	BR R11	return
0000257C				1525+RE28	DC OF	xl16 expected result
0000257C				1526+	DROP R5	
0000257C	FCF0F4F8 FCF0F4F8			1527	DC XL16' FCF0F4F8FCF0F4F8 FCF0F4F8FCF0F4F8'	result t
00002584	FCF0F4F8 FCF0F4F8					
0000258C	F0F0F0F0 F0F0F0F0			1528	DC XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002594	F0F0F0F0 F0F0F0F0					
0000259C	00010203 04050607			1529	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000025A4	08090A0B 0C0D0E0F					
000025AC	0F0F0F0F 0F0F0F0F			1530	DC XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000025B4	0F0F0F0F 0F0F0F0F					
				1531		
000025C0				1532	VRI_D VERIM, 248, 2	248-8 right
000025C0		000025C0		1533+	DS OFD	
000025C0	00002608			1534+	USING *, R5	base for test data and test routine
000025C4	001D			1535+T29	DC A(X29)	address of test routine
000025C6	00			1536+	DC H' 29'	test number
000025C7	F8			1537+	DC X' 00'	
000025C8	02			1538+	DC HL1' 248'	i4 field
000025C8				1539+	DC HL1' 2'	m5 field
000025C9	E5C5D9C9 D4404040			1540+	DC CL8' VERIM	instruction name
000025D4	0000264C			1541+	DC A(RE29+16)	address of v1 source
000025D8	0000265C			1542+	DC A(RE29+32)	address of v2 source
000025DC	0000266C			1543+	DC A(RE29+48)	address of v3 source
000025E0	00000010			1544+	DC A(16)	result length
000025E4	0000263C			1545+REA29	DC A(RE29)	result address
000025E8	00000000 00000000			1546+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1568 *Doubleword		
				1569	VRI_D VERIM, 0, 3	
00002680				1570+	DS OFD	
00002680		00002680		1571+	USING *, R5	base for test data and test routine
00002680	000026C8			1572+T30	DC A(X30)	address of test routine
00002684	001E			1573+	DC H' 30'	test number
00002686	00			1574+	DC X' 00'	
00002687	00			1575+	DC HL1' 0'	i4 field
00002688	03			1576+	DC HL1' 3'	m5 field
00002689	E5C5D9C9 D4404040			1577+	DC CL8' VERIM	instruction name
00002694	0000270C			1578+	DC A(RE30+16)	address of v1 source
00002698	0000271C			1579+	DC A(RE30+32)	address of v2 source
0000269C	0000272C			1580+	DC A(RE30+48)	address of v3 source
000026A0	00000010			1581+	DC A(16)	result length
000026A4	000026FC			1582+REA30	DC A(RE30)	result address
000026A8	00000000 00000000			1583+	DS FD	gap
000026B0	00000000 00000000			1584+V1030	DS XL16	V1 output
000026B8	00000000 00000000					
000026C0	00000000 00000000			1585+	DS FD	gap
				1586+*		
000026C8				1587+X30	DS OF	
000026C8	E310 5014 0014		00000014	1588+	LGF R1, V1ADDR	load v1 source
000026CE	E751 0000 0806		00000000	1589+	VL v21, 0(R1)	use v21 to test decoder
000026D4	E310 5018 0014		00000018	1590+	LGF R1, V2ADDR	load v2 source
000026DA	E761 0000 0806		00000000	1591+	VL v22, 0(R1)	use v22 to test decoder
000026E0	E310 501C 0014		0000001C	1592+	LGF R1, V3ADDR	load v3 source
000026E6	E771 0000 0806		00000000	1593+	VL v23, 0(R1)	use v23 to test decoder
000026EC	E756 7000 3E72			1594+	VERIM V21, V22, V23, 0, 3	test instruction
000026F2	E750 5030 080E		000026B0	1595+	VST V21, V1030	save v1 output
000026F8	07FB			1596+	BR R11	return
000026FC				1597+RE30	DC OF	xl16 expected result
000026FC				1598+	DROP R5	
000026FC	F0F1F2F3 F4F5F6F7			1599	DC XL16' F0F1F2F3F4F5F6F7 F8F9FAFBFCFDFEFF'	result t
00002704	F8F9FAFB FCFDFEFF					
0000270C	F0F0F0F0 F0F0F0F0			1600	DC XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002714	F0F0F0F0 F0F0F0F0					
0000271C	00010203 04050607			1601	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002724	08090A0B 0C0D0E0F					
0000272C	0F0F0F0F 0F0F0F0F			1602	DC XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002734	0F0F0F0F 0F0F0F0F					
				1603		
				1604	VRI_D VERIM, 1, 3	
00002740				1605+	DS OFD	
00002740		00002740		1606+	USING *, R5	base for test data and test routine
00002740	00002788			1607+T31	DC A(X31)	address of test routine
00002744	001F			1608+	DC H' 31'	test number
00002746	00			1609+	DC X' 00'	
00002747	01			1610+	DC HL1' 1'	i4 field
00002748	03			1611+	DC HL1' 3'	m5 field
00002749	E5C5D9C9 D4404040			1612+	DC CL8' VERIM	instruction name
00002754	000027CC			1613+	DC A(RE31+16)	address of v1 source
00002758	000027DC			1614+	DC A(RE31+32)	address of v2 source
0000275C	000027EC			1615+	DC A(RE31+48)	address of v3 source
00002760	00000010			1616+	DC A(16)	result length
00002764	000027BC			1617+REA31	DC A(RE31)	result address
00002768	00000000 00000000			1618+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002770	00000000 00000000			1619+V1031	DS	XL16	V1 output
00002778	00000000 00000000						
00002780	00000000 00000000			1620+	DS	FD	gap
				1621+*			
00002788				1622+X31	DS	0F	
00002788	E310 5014 0014		00000014	1623+	LGF	R1, V1ADDR	load v1 source
0000278E	E751 0000 0806		00000000	1624+	VL	v21, 0(R1)	use v21 to test decoder
00002794	E310 5018 0014		00000018	1625+	LGF	R1, V2ADDR	load v2 source
0000279A	E761 0000 0806		00000000	1626+	VL	v22, 0(R1)	use v22 to test decoder
000027A0	E310 501C 0014		0000001C	1627+	LGF	R1, V3ADDR	load v3 source
000027A6	E771 0000 0806		00000000	1628+	VL	v23, 0(R1)	use v23 to test decoder
000027AC	E756 7001 3E72			1629+	VERIM	V21, V22, V23, 1, 3	test instruction
000027B2	E750 5030 080E		00002770	1630+	VST	V21, V1031	save v1 output
000027B8	07FB			1631+	BR	R11	return
000027BC				1632+RE31	DC	0F	xl16 expected result
000027BC				1633+	DROP	R5	
000027BC	F0F2F4F6 F8FAFCFE			1634	DC	XL16' F0F2F4F6F8FAFCFE F0F2F4F6F8FAFCFE'	result t
000027C4	F0F2F4F6 F8FAFCFE						
000027CC	F0F0F0F0 F0F0F0F0			1635	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
000027D4	F0F0F0F0 F0F0F0F0						
000027DC	00010203 04050607			1636	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000027E4	08090A0B 0C0D0E0F						
000027EC	0F0F0F0F 0F0F0F0F			1637	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000027F4	0F0F0F0F 0F0F0F0F						
				1638			
				1639	VRI_D	VERIM, 2, 3	
00002800				1640+	DS	0FD	
00002800		00002800		1641+	USING	*, R5	base for test data and test routine
00002800	00002848			1642+T32	DC	A(X32)	address of test routine
00002804	0020			1643+	DC	H' 32'	test number
00002806	00			1644+	DC	X' 00'	
00002807	02			1645+	DC	HL1' 2'	i4 field
00002808	03			1646+	DC	HL1' 3'	m5 field
00002809	E5C5D9C9 D4404040			1647+	DC	CL8' VERIM	instruction name
00002814	0000288C			1648+	DC	A(RE32+16)	address of v1 source
00002818	0000289C			1649+	DC	A(RE32+32)	address of v2 source
0000281C	000028AC			1650+	DC	A(RE32+48)	address of v3 source
00002820	00000010			1651+	DC	A(16)	result length
00002824	0000287C			1652+REA32	DC	A(RE32)	result address
00002828	00000000 00000000			1653+	DS	FD	gap
00002830	00000000 00000000			1654+V1032	DS	XL16	V1 output
00002838	00000000 00000000						
00002840	00000000 00000000			1655+	DS	FD	gap
				1656+*			
00002848				1657+X32	DS	0F	
00002848	E310 5014 0014		00000014	1658+	LGF	R1, V1ADDR	load v1 source
0000284E	E751 0000 0806		00000000	1659+	VL	v21, 0(R1)	use v21 to test decoder
00002854	E310 5018 0014		00000018	1660+	LGF	R1, V2ADDR	load v2 source
0000285A	E761 0000 0806		00000000	1661+	VL	v22, 0(R1)	use v22 to test decoder
00002860	E310 501C 0014		0000001C	1662+	LGF	R1, V3ADDR	load v3 source
00002866	E771 0000 0806		00000000	1663+	VL	v23, 0(R1)	use v23 to test decoder
0000286C	E756 7002 3E72			1664+	VERIM	V21, V22, V23, 2, 3	test instruction
00002872	E750 5030 080E		00002830	1665+	VST	V21, V1032	save v1 output
00002878	07FB			1666+	BR	R11	return
0000287C				1667+RE32	DC	0F	xl16 expected result
0000287C				1668+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000287C	F0F4F8FC F0F4F8FC			1669	DC	XL16' F0F4F8FCF0F4F8FC F0F4F8FCF0F4F8FC'	result
00002884	F0F4F8FC F0F4F8FC						
0000288C	F0F0F0F0 F0F0F0F0			1670	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002894	F0F0F0F0 F0F0F0F0						
0000289C	00010203 04050607			1671	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000028A4	08090A0B 0C0D0E0F						
000028AC	0F0F0F0F 0F0F0F0F			1672	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
000028B4	0F0F0F0F 0F0F0F0F						
				1673			
				1674	VRI_D	VERIM, 5, 3	
000028C0				1675+	DS	0FD	
000028C0		000028C0		1676+	USING	*, R5	base for test data and test routine
000028C0	00002908			1677+T33	DC	A(X33)	address of test routine
000028C4	0021			1678+	DC	H' 33'	test number
000028C6	00			1679+	DC	X' 00'	
000028C7	05			1680+	DC	HL1' 5'	i4 field
000028C8	03			1681+	DC	HL1' 3'	m5 field
000028C9	E5C5D9C9 D4404040			1682+	DC	CL8' VERIM	instruction name
000028D4	0000294C			1683+	DC	A(RE33+16)	address of v1 source
000028D8	0000295C			1684+	DC	A(RE33+32)	address of v2 source
000028DC	0000296C			1685+	DC	A(RE33+48)	address of v3 source
000028E0	00000010			1686+	DC	A(16)	result length
000028E4	0000293C			1687+REA33	DC	A(RE33)	result address
000028E8	00000000 00000000			1688+	DS	FD	gap
000028F0	00000000 00000000			1689+V1033	DS	XL16	V1 output
000028F8	00000000 00000000						
00002900	00000000 00000000			1690+	DS	FD	gap
				1691+*			
00002908				1692+X33	DS	0F	
00002908	E310 5014 0014		00000014	1693+	LGF	R1, V1ADDR	load v1 source
0000290E	E751 0000 0806		00000000	1694+	VL	v21, 0(R1)	use v21 to test decoder
00002914	E310 5018 0014		00000018	1695+	LGF	R1, V2ADDR	load v2 source
0000291A	E761 0000 0806		00000000	1696+	VL	v22, 0(R1)	use v22 to test decoder
00002920	E310 501C 0014		0000001C	1697+	LGF	R1, V3ADDR	load v3 source
00002926	E771 0000 0806		00000000	1698+	VL	v23, 0(R1)	use v23 to test decoder
0000292C	E756 7005 3E72			1699+	VERIM	V21, V22, V23, 5, 3	test instruction
00002932	E750 5030 080E		000028F0	1700+	VST	V21, V1033	save v1 output
00002938	07FB			1701+	BR	R11	return
0000293C				1702+RE33	DC	0F	xl16 expected result
0000293C				1703+	DROP	R5	
0000293C	F0F0F0F0 F0F0F0F0			1704	DC	XL16' F0F0F0F0F0F0F0F0 F1F1F1F1F1F1F1F1'	result
00002944	F1F1F1F1 F1F1F1F1						
0000294C	F0F0F0F0 F0F0F0F0			1705	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002954	F0F0F0F0 F0F0F0F0						
0000295C	00010203 04050607			1706	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002964	08090A0B 0C0D0E0F						
0000296C	0F0F0F0F 0F0F0F0F			1707	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002974	0F0F0F0F 0F0F0F0F						
				1708			
				1709	VRI_D	VERIM, 7, 3	
00002980				1710+	DS	0FD	
00002980		00002980		1711+	USING	*, R5	base for test data and test routine
00002980	000029C8			1712+T34	DC	A(X34)	address of test routine
00002984	0022			1713+	DC	H' 34'	test number
00002986	00			1714+	DC	X' 00'	
00002987	07			1715+	DC	HL1' 7'	i4 field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002988	03			1716+	DC	HL1' 3'	m5 field
00002989	E5C5D9C9 D4404040			1717+	DC	CL8' VERIM	instruction name
00002994	00002A0C			1718+	DC	A(RE34+16)	address of v1 source
00002998	00002A1C			1719+	DC	A(RE34+32)	address of v2 source
0000299C	00002A2C			1720+	DC	A(RE34+48)	address of v3 source
000029A0	00000010			1721+	DC	A(16)	result length
000029A4	000029FC			1722+REA34	DC	A(RE34)	result address
000029A8	00000000 00000000			1723+	DS	FD	gap
000029B0	00000000 00000000			1724+V1034	DS	XL16	V1 output
000029B8	00000000 00000000						
000029C0	00000000 00000000			1725+	DS	FD	gap
				1726+*			
000029C8				1727+X34	DS	0F	
000029C8	E310 5014 0014		00000014	1728+	LGF	R1, V1ADDR	load v1 source
000029CE	E751 0000 0806		00000000	1729+	VL	v21, 0(R1)	use v21 to test decoder
000029D4	E310 5018 0014		00000018	1730+	LGF	R1, V2ADDR	load v2 source
000029DA	E761 0000 0806		00000000	1731+	VL	v22, 0(R1)	use v22 to test decoder
000029E0	E310 501C 0014		0000001C	1732+	LGF	R1, V3ADDR	load v3 source
000029E6	E771 0000 0806		00000000	1733+	VL	v23, 0(R1)	use v23 to test decoder
000029EC	E756 7007 3E72			1734+	VERIM	V21, V22, V23, 7, 3	test instruction
000029F2	E750 5030 080E		000029B0	1735+	VST	V21, V1034	save v1 output
000029F8	07FB			1736+	BR	R11	return
000029FC				1737+RE34	DC	0F	xl16 expected result
000029FC				1738+	DROP	R5	
000029FC	F0F1F1F2 F2F3F3F0			1739	DC	XL16' F0F1F1F2F2F3F3F0 F4F5F5F6F6F7F7F4'	result t
00002A04	F4F5F5F6 F6F7F7F4						
00002A0C	F0F0F0F0 F0F0F0F0			1740	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002A14	F0F0F0F0 F0F0F0F0						
00002A1C	00010203 04050607			1741	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002A24	08090A0B 0C0D0E0F						
00002A2C	0F0F0F0F 0F0F0F0F			1742	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002A34	0F0F0F0F 0F0F0F0F						
				1743			
				1744	VRI_D	VERIM, 255, 3	255->1 right
00002A40				1745+	DS	0FD	
00002A40		00002A40		1746+	USING	*, R5	base for test data and test routine
00002A40	00002A88			1747+T35	DC	A(X35)	address of test routine
00002A44	0023			1748+	DC	H' 35'	test number
00002A46	00			1749+	DC	X' 00'	
00002A47	FF			1750+	DC	HL1' 255'	i4 field
00002A48	03			1751+	DC	HL1' 3'	m5 field
00002A49	E5C5D9C9 D4404040			1752+	DC	CL8' VERIM	instruction name
00002A54	00002ACC			1753+	DC	A(RE35+16)	address of v1 source
00002A58	00002ADC			1754+	DC	A(RE35+32)	address of v2 source
00002A5C	00002AEC			1755+	DC	A(RE35+48)	address of v3 source
00002A60	00000010			1756+	DC	A(16)	result length
00002A64	00002ABC			1757+REA35	DC	A(RE35)	result address
00002A68	00000000 00000000			1758+	DS	FD	gap
00002A70	00000000 00000000			1759+V1035	DS	XL16	V1 output
00002A78	00000000 00000000						
00002A80	00000000 00000000			1760+	DS	FD	gap
				1761+*			
00002A88				1762+X35	DS	0F	
00002A88	E310 5014 0014		00000014	1763+	LGF	R1, V1ADDR	load v1 source
00002A8E	E751 0000 0806		00000000	1764+	VL	v21, 0(R1)	use v21 to test decoder
00002A94	E310 5018 0014		00000018	1765+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002A9A	E761 0000 0806		00000000	1766+	VL	v22, 0(R1)	use v22 to test decoder
00002AA0	E310 501C 0014		0000001C	1767+	LGF	R1, V3ADDR	load v3 source
00002AA6	E771 0000 0806		00000000	1768+	VL	v23, 0(R1)	use v23 to test decoder
00002AAC	E756 70FF 3E72			1769+	VERIM	V21, V22, V23, 255, 3	test instruction
00002AB2	E750 5030 080E		00002A70	1770+	VST	V21, V1035	save v1 output
00002AB8	07FB			1771+	BR	R11	return
00002ABC				1772+RE35	DC	0F	xl16 expected result
00002ABC				1773+	DROP	R5	
00002ABC	F0F0F1F1 F2F2F3F3			1774	DC	XL16' F0F0F1F1F2F2F3F3 F4F4F5F5F6F6F7F7'	result t
00002AC4	F4F4F5F5 F6F6F7F7						
00002ACC	F0F0F0F0 F0F0F0F0			1775	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002AD4	F0F0F0F0 F0F0F0F0						
00002ADC	00010203 04050607			1776	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002AE4	08090A0B 0C0D0E0F						
00002AEC	0F0F0F0F 0F0F0F0F			1777	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002AF4	0F0F0F0F 0F0F0F0F						
				1778			
00002B00				1779	VRI_D	VERIM, 254, 3	254->2 right
00002B00		00002B00		1780+	DS	0FD	
00002B00	00002B48			1781+	USING	*, R5	base for test data and test routine
00002B04	0024			1782+T36	DC	A(X36)	address of test routine
00002B06	00			1783+	DC	H' 36'	test number
00002B06	00			1784+	DC	X' 00'	
00002B07	FE			1785+	DC	HL1' 254'	i4 field
00002B08	03			1786+	DC	HL1' 3'	m5 field
00002B09	E5C5D9C9 D4404040			1787+	DC	CL8' VERIM	instruction name
00002B14	00002B8C			1788+	DC	A(RE36+16)	address of v1 source
00002B18	00002B9C			1789+	DC	A(RE36+32)	address of v2 source
00002B1C	00002BAC			1790+	DC	A(RE36+48)	address of v3 source
00002B20	00000010			1791+	DC	A(16)	result length
00002B24	00002B7C			1792+REA36	DC	A(RE36)	result address
00002B28	00000000 00000000			1793+	DS	FD	gap
00002B30	00000000 00000000			1794+V1036	DS	XL16	V1 output
00002B38	00000000 00000000						
00002B40	00000000 00000000			1795+	DS	FD	gap
				1796+*			
00002B48				1797+X36	DS	0F	
00002B48	E310 5014 0014		00000014	1798+	LGF	R1, V1ADDR	load v1 source
00002B4E	E751 0000 0806		00000000	1799+	VL	v21, 0(R1)	use v21 to test decoder
00002B54	E310 5018 0014		00000018	1800+	LGF	R1, V2ADDR	load v2 source
00002B5A	E761 0000 0806		00000000	1801+	VL	v22, 0(R1)	use v22 to test decoder
00002B60	E310 501C 0014		0000001C	1802+	LGF	R1, V3ADDR	load v3 source
00002B66	E771 0000 0806		00000000	1803+	VL	v23, 0(R1)	use v23 to test decoder
00002B6C	E756 70FE 3E72			1804+	VERIM	V21, V22, V23, 254, 3	test instruction
00002B72	E750 5030 080E		00002B30	1805+	VST	V21, V1036	save v1 output
00002B78	07FB			1806+	BR	R11	return
00002B7C				1807+RE36	DC	0F	xl16 expected result
00002B7C				1808+	DROP	R5	
00002B7C	F0F0F0F0 F1F1F1F1			1809	DC	XL16' F0F0F0F0F1F1F1F1 F2F2F2F2F3F3F3F3'	result t
00002B84	F2F2F2F2 F3F3F3F3						
00002B8C	F0F0F0F0 F0F0F0F0			1810	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002B94	F0F0F0F0 F0F0F0F0						
00002B9C	00010203 04050607			1811	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002BA4	08090A0B 0C0D0E0F						
00002BAC	0F0F0F0F 0F0F0F0F			1812	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002BB4	0F0F0F0F 0F0F0F0F						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				1813		
				1814	VRI_D VERIM, 250, 3	250->6 right
00002BC0				1815+	DS OFD	
00002BC0		00002BC0		1816+	USING *, R5	base for test data and test routine
00002BC0	00002C08			1817+T37	DC A(X37)	address of test routine
00002BC4	0025			1818+	DC H' 37'	test number
00002BC6	00			1819+	DC X' 00'	
00002BC7	FA			1820+	DC HL1' 250'	i4 field
00002BC8	03			1821+	DC HL1' 3'	m5 field
00002BC9	E5C5D9C9 D4404040			1822+	DC CL8' VERIM	instruction name
00002BD4	00002C4C			1823+	DC A(RE37+16)	address of v1 source
00002BD8	00002C5C			1824+	DC A(RE37+32)	address of v2 source
00002BDC	00002C6C			1825+	DC A(RE37+48)	address of v3 source
00002BE0	00000010			1826+	DC A(16)	result length
00002BE4	00002C3C			1827+REA37	DC A(RE37)	result address
00002BE8	00000000 00000000			1828+	DS FD	gap
00002BF0	00000000 00000000			1829+V1037	DS XL16	V1 output
00002BF8	00000000 00000000					
00002C00	00000000 00000000			1830+	DS FD	gap
				1831+*		
00002C08				1832+X37	DS OF	
00002C08	E310 5014 0014		00000014	1833+	LGF R1, V1ADDR	load v1 source
00002C0E	E751 0000 0806		00000000	1834+	VL v21, 0(R1)	use v21 to test decoder
00002C14	E310 5018 0014		00000018	1835+	LGF R1, V2ADDR	load v2 source
00002C1A	E761 0000 0806		00000000	1836+	VL v22, 0(R1)	use v22 to test decoder
00002C20	E310 501C 0014		0000001C	1837+	LGF R1, V3ADDR	load v3 source
00002C26	E771 0000 0806		00000000	1838+	VL v23, 0(R1)	use v23 to test decoder
00002C2C	E756 70FA 3E72			1839+	VERIM V21, V22, V23, 250, 3	test instruction
00002C32	E750 5030 080E		00002BF0	1840+	VST V21, V1037	save v1 output
00002C38	07FB			1841+	BR R11	return
00002C3C				1842+RE37	DC OF	xl16 expected result
00002C3C				1843+	DROP R5	
00002C3C	FCF0F4F8 FCF0F4F8			1844	DC XL16' FCF0F4F8FCF0F4F8 FCF0F4F8FCF0F4F8'	result t
00002C44	FCF0F4F8 FCF0F4F8					
00002C4C	F0F0F0F0 F0F0F0F0			1845	DC XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002C54	F0F0F0F0 F0F0F0F0					
00002C5C	00010203 04050607			1846	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002C64	08090A0B 0C0D0E0F					
00002C6C	0F0F0F0F 0F0F0F0F			1847	DC XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002C74	0F0F0F0F 0F0F0F0F					
				1848		
00002C80				1849	VRI_D VERIM, 248, 3	248-8 right
00002C80		00002C80		1850+	DS OFD	
00002C80	00002CC8			1851+	USING *, R5	base for test data and test routine
00002C84	0026			1852+T38	DC A(X38)	address of test routine
00002C86	00			1853+	DC H' 38'	test number
00002C86	00			1854+	DC X' 00'	
00002C87	F8			1855+	DC HL1' 248'	i4 field
00002C88	03			1856+	DC HL1' 3'	m5 field
00002C89	E5C5D9C9 D4404040			1857+	DC CL8' VERIM	instruction name
00002C94	00002D0C			1858+	DC A(RE38+16)	address of v1 source
00002C98	00002D1C			1859+	DC A(RE38+32)	address of v2 source
00002C9C	00002D2C			1860+	DC A(RE38+48)	address of v3 source
00002CA0	00000010			1861+	DC A(16)	result length
00002CA4	00002CFC			1862+REA38	DC A(RE38)	result address
00002CA8	00000000 00000000			1863+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002CB0	00000000 00000000			1864+V1038	DS	XL16	V1 output
00002CB8	00000000 00000000						
00002CC0	00000000 00000000			1865+	DS	FD	gap
				1866+*			
00002CC8				1867+X38	DS	0F	
00002CC8	E310 5014 0014		00000014	1868+	LGF	R1, V1ADDR	load v1 source
00002CCE	E751 0000 0806		00000000	1869+	VL	v21, 0(R1)	use v21 to test decoder
00002CD4	E310 5018 0014		00000018	1870+	LGF	R1, V2ADDR	load v2 source
00002CDA	E761 0000 0806		00000000	1871+	VL	v22, 0(R1)	use v22 to test decoder
00002CE0	E310 501C 0014		0000001C	1872+	LGF	R1, V3ADDR	load v3 source
00002CE6	E771 0000 0806		00000000	1873+	VL	v23, 0(R1)	use v23 to test decoder
00002CEC	E756 70F8 3E72			1874+	VERIM	V21, V22, V23, 248, 3	test instruction
00002CF2	E750 5030 080E		00002CB0	1875+	VST	V21, V1038	save v1 output
00002CF8	07FB			1876+	BR	R11	return
00002CFC				1877+RE38	DC	0F	xl16 expected result
00002CFC				1878+	DROP	R5	
00002CFC	F7F0F1F2 F3F4F5F6			1879	DC	XL16' F7F0F1F2F3F4F5F6 FFF8F9FAFBFCFDFE'	result t
00002D04	FFF8F9FA FBFCFDFE						
00002D0C	F0F0F0F0 F0F0F0F0			1880	DC	XL16' F0F0F0F0F0F0F0F0 F0F0F0F0F0F0F0F0'	v1
00002D14	F0F0F0F0 F0F0F0F0						
00002D1C	00010203 04050607			1881	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002D24	08090A0B 0C0D0E0F						
00002D2C	0F0F0F0F 0F0F0F0F			1882	DC	XL16' 0F0F0F0F0F0F0F0F 0F0F0F0F0F0F0F0F'	v3
00002D34	0F0F0F0F 0F0F0F0F						
				1883			
				1884 *			
				1885 * case 2			
				1886 *			
				1887 *Byte			
				1888	VRI_D	VERIM, 0, 0	
00002D40				1889+	DS	0FD	
00002D40		00002D40		1890+	USING	*, R5	base for test data and test routine
00002D40	00002D88			1891+T39	DC	A(X39)	address of test routine
00002D44	0027			1892+	DC	H' 39'	test number
00002D46	00			1893+	DC	X' 00'	
00002D47	00			1894+	DC	HL1' 0'	i4 field
00002D48	00			1895+	DC	HL1' 0'	m5 field
00002D49	E5C5D9C9 D4404040			1896+	DC	CL8' VERIM	instruction name
00002D54	00002DCC			1897+	DC	A(RE39+16)	address of v1 source
00002D58	00002DDC			1898+	DC	A(RE39+32)	address of v2 source
00002D5C	00002DEC			1899+	DC	A(RE39+48)	address of v3 source
00002D60	00000010			1900+	DC	A(16)	result length
00002D64	00002DBC			1901+REA39	DC	A(RE39)	result address
00002D68	00000000 00000000			1902+	DS	FD	gap
00002D70	00000000 00000000			1903+V1039	DS	XL16	V1 output
00002D78	00000000 00000000						
00002D80	00000000 00000000			1904+	DS	FD	gap
				1905+*			
00002D88				1906+X39	DS	0F	
00002D88	E310 5014 0014		00000014	1907+	LGF	R1, V1ADDR	load v1 source
00002D8E	E751 0000 0806		00000000	1908+	VL	v21, 0(R1)	use v21 to test decoder
00002D94	E310 5018 0014		00000018	1909+	LGF	R1, V2ADDR	load v2 source
00002D9A	E761 0000 0806		00000000	1910+	VL	v22, 0(R1)	use v22 to test decoder
00002DA0	E310 501C 0014		0000001C	1911+	LGF	R1, V3ADDR	load v3 source
00002DA6	E771 0000 0806		00000000	1912+	VL	v23, 0(R1)	use v23 to test decoder
00002DAC	E756 7000 0E72			1913+	VERIM	V21, V22, V23, 0, 0	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002DB2	E750 5030 080E		00002D70	1914+	VST	V21, V1039	save v1 output	
00002DB8	07FB			1915+	BR	R11	return	
00002DBC				1916+RE39	DC	0F	xl16 expected result	
00002DBC				1917+	DROP	R5		
00002DBC	00010203 04050607			1918	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	result t	
00002DC4	08090A0B 0C0D0E0F							
00002DCC	00010203 04050607			1919	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00002DD4	08090A0B 0C0D0E0F							
00002DDC	00010203 04050607			1920	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00002DE4	08090A0B 0C0D0E0F							
00002DEC	00000000 00000000			1921	DC	XL16' 0000000000000000 0000000000000000'	v3	
00002DF4	00000000 00000000							
				1922				
				1923	VRI_D	VERIM, 1, 0		
00002E00				1924+	DS	0FD		
00002E00		00002E00		1925+	USING	*, R5	base for test data and test routine	
00002E00	00002E48			1926+T40	DC	A(X40)	address of test routine	
00002E04	0028			1927+	DC	H' 40'	test number	
00002E06	00			1928+	DC	X' 00'		
00002E07	01			1929+	DC	HL1' 1'	i4 field	
00002E08	00			1930+	DC	HL1' 0'	m5 field	
00002E09	E5C5D9C9 D4404040			1931+	DC	CL8' VERIM	instruction name	
00002E14	00002E8C			1932+	DC	A(RE40+16)	address of v1 source	
00002E18	00002E9C			1933+	DC	A(RE40+32)	address of v2 source	
00002E1C	00002EAC			1934+	DC	A(RE40+48)	address of v3 source	
00002E20	00000010			1935+	DC	A(16)	result length	
00002E24	00002E7C			1936+REA40	DC	A(RE40)	result address	
00002E28	00000000 00000000			1937+	DS	FD	gap	
00002E30	00000000 00000000			1938+V1040	DS	XL16	V1 output	
00002E38	00000000 00000000							
00002E40	00000000 00000000			1939+	DS	FD	gap	
				1940+*				
00002E48				1941+X40	DS	0F		
00002E48	E310 5014 0014		00000014	1942+	LGF	R1, V1ADDR	load v1 source	
00002E4E	E751 0000 0806		00000000	1943+	VL	v21, 0(R1)	use v21 to test decoder	
00002E54	E310 5018 0014		00000018	1944+	LGF	R1, V2ADDR	load v2 source	
00002E5A	E761 0000 0806		00000000	1945+	VL	v22, 0(R1)	use v22 to test decoder	
00002E60	E310 501C 0014		0000001C	1946+	LGF	R1, V3ADDR	load v3 source	
00002E66	E771 0000 0806		00000000	1947+	VL	v23, 0(R1)	use v23 to test decoder	
00002E6C	E756 7001 0E72			1948+	VERIM	V21, V22, V23, 1, 0	test instruction	
00002E72	E750 5030 080E		00002E30	1949+	VST	V21, V1040	save v1 output	
00002E78	07FB			1950+	BR	R11	return	
00002E7C				1951+RE40	DC	0F	xl16 expected result	
00002E7C				1952+	DROP	R5		
00002E7C	00020002 04060406			1953	DC	XL16' 0002000204060406 080A080A0C0E0C0E'	result t	
00002E84	080A080A 0C0E0C0E							
00002E8C	00010203 04050607			1954	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00002E94	08090A0B 0C0D0E0F							
00002E9C	00010203 04050607			1955	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00002EA4	08090A0B 0C0D0E0F							
00002EAC	C3C3C3C3 C3C3C3C3			1956	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00002EB4	C3C3C3C3 C3C3C3C3							
				1957				
				1958	VRI_D	VERIM, 2, 0		
00002EC0				1959+	DS	0FD		
00002EC0		00002EC0		1960+	USING	*, R5	base for test data and test routine	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00002EC0	00002F08			1961+T41	DC	A(X41)	address of test routine
00002EC4	0029			1962+	DC	H' 41'	test number
00002EC6	00			1963+	DC	X' 00'	
00002EC7	02			1964+	DC	HL1' 2'	i4 field
00002EC8	00			1965+	DC	HL1' 0'	m5 field
00002EC9	E5C5D9C9 D4404040			1966+	DC	CL8' VERIM	instruction name
00002ED4	00002F4C			1967+	DC	A(RE41+16)	address of v1 source
00002ED8	00002F5C			1968+	DC	A(RE41+32)	address of v2 source
00002EDC	00002F6C			1969+	DC	A(RE41+48)	address of v3 source
00002EE0	00000010			1970+	DC	A(16)	result length
00002EE4	00002F3C			1971+REA41	DC	A(RE41)	result address
00002EE8	00000000 00000000			1972+	DS	FD	gap
00002EF0	00000000 00000000			1973+V1041	DS	XL16	V1 output
00002EF8	00000000 00000000						
00002F00	00000000 00000000			1974+	DS	FD	gap
				1975+*			
00002F08				1976+X41	DS	0F	
00002F08	E310 5014 0014		00000014	1977+	LGF	R1, V1ADDR	load v1 source
00002F0E	E751 0000 0806		00000000	1978+	VL	v21, 0(R1)	use v21 to test decoder
00002F14	E310 5018 0014		00000018	1979+	LGF	R1, V2ADDR	load v2 source
00002F1A	E761 0000 0806		00000000	1980+	VL	v22, 0(R1)	use v22 to test decoder
00002F20	E310 501C 0014		0000001C	1981+	LGF	R1, V3ADDR	load v3 source
00002F26	E771 0000 0806		00000000	1982+	VL	v23, 0(R1)	use v23 to test decoder
00002F2C	E756 7002 0E72			1983+	VERIM	V21, V22, V23, 2, 0	test instruction
00002F32	E750 5030 080E		00002EF0	1984+	VST	V21, V1041	save v1 output
00002F38	07FB			1985+	BR	R11	return
00002F3C				1986+RE41	DC	0F	xl16 expected result
00002F3C				1987+	DROP	R5	
00002F3C	00000000 04040404			1988	DC	XL16' 0000000004040404 080808080C0C0C0C'	result t
00002F44	08080808 0C0C0C0C						
00002F4C	00010203 04050607			1989	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00002F54	08090A0B 0C0D0E0F						
00002F5C	00010203 04050607			1990	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00002F64	08090A0B 0C0D0E0F						
00002F6C	C3C3C3C3 C3C3C3C3			1991	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00002F74	C3C3C3C3 C3C3C3C3						
				1992			
				1993	VRI_D	VERIM, 5, 0	
00002F80				1994+	DS	0FD	
00002F80		00002F80		1995+	USING	*, R5	base for test data and test routine
00002F80	00002FC8			1996+T42	DC	A(X42)	address of test routine
00002F84	002A			1997+	DC	H' 42'	test number
00002F86	00			1998+	DC	X' 00'	
00002F87	05			1999+	DC	HL1' 5'	i4 field
00002F88	00			2000+	DC	HL1' 0'	m5 field
00002F89	E5C5D9C9 D4404040			2001+	DC	CL8' VERIM	instruction name
00002F94	0000300C			2002+	DC	A(RE42+16)	address of v1 source
00002F98	0000301C			2003+	DC	A(RE42+32)	address of v2 source
00002F9C	0000302C			2004+	DC	A(RE42+48)	address of v3 source
00002FA0	00000010			2005+	DC	A(16)	result length
00002FA4	00002FFC			2006+REA42	DC	A(RE42)	result address
00002FA8	00000000 00000000			2007+	DS	FD	gap
00002FB0	00000000 00000000			2008+V1042	DS	XL16	V1 output
00002FB8	00000000 00000000						
00002FC0	00000000 00000000			2009+	DS	FD	gap
				2010+*			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00002FC8				2011+X42	DS	0F		
00002FC8	E310 5014 0014		00000014	2012+	LGF	R1, V1ADDR	load v1 source	
00002FCE	E751 0000 0806		00000000	2013+	VL	v21, 0(R1)	use v21 to test decoder	
00002FD4	E310 5018 0014		00000018	2014+	LGF	R1, V2ADDR	load v2 source	
00002FDA	E761 0000 0806		00000000	2015+	VL	v22, 0(R1)	use v22 to test decoder	
00002FE0	E310 501C 0014		0000001C	2016+	LGF	R1, V3ADDR	load v3 source	
00002FE6	E771 0000 0806		00000000	2017+	VL	v23, 0(R1)	use v23 to test decoder	
00002FEC	E756 7005 0E72			2018+	VERIM	V21, V22, V23, 5, 0	test instruction	
00002FF2	E750 5030 080E		00002FB0	2019+	VST	V21, V1042	save v1 output	
00002FF8	07FB			2020+	BR	R11	return	
00002FFC				2021+RE42	DC	0F	xl16 expected result	
00002FFC				2022+	DROP	R5		
00002FFC	00004040 8484C4C4			2023	DC	XL16' 000040408484C4C4 090949498D8DCDCD'	result t	
00003004	09094949 8D8DCDCD							
0000300C	00010203 04050607			2024	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003014	08090A0B 0C0D0E0F							
0000301C	00010203 04050607			2025	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00003024	08090A0B 0C0D0E0F							
0000302C	C3C3C3C3 C3C3C3C3			2026	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00003034	C3C3C3C3 C3C3C3C3							
				2027				
00003040				2028	VRI_D	VERIM, 7, 0		
00003040		00003040		2029+	DS	0FD		
00003040	00003088			2030+	USING	*, R5	base for test data and test routine	
00003044	002B			2031+T43	DC	A(X43)	address of test routine	
00003046	00			2032+	DC	H' 43'	test number	
00003047	07			2033+	DC	X' 00'		
00003048	00			2034+	DC	HL1' 7'	i4 field	
00003048	00			2035+	DC	HL1' 0'	m5 field	
00003049	E5C5D9C9 D4404040			2036+	DC	CL8' VERIM	instruction name	
00003054	000030CC			2037+	DC	A(RE43+16)	address of v1 source	
00003058	000030DC			2038+	DC	A(RE43+32)	address of v2 source	
0000305C	000030EC			2039+	DC	A(RE43+48)	address of v3 source	
00003060	00000010			2040+	DC	A(16)	result length	
00003064	000030BC			2041+REA43	DC	A(RE43)	result address	
00003068	00000000 00000000			2042+	DS	FD	gap	
00003070	00000000 00000000			2043+V1043	DS	XL16	V1 output	
00003078	00000000 00000000							
00003080	00000000 00000000			2044+	DS	FD	gap	
				2045+*				
00003088				2046+X43	DS	0F		
00003088	E310 5014 0014		00000014	2047+	LGF	R1, V1ADDR	load v1 source	
0000308E	E751 0000 0806		00000000	2048+	VL	v21, 0(R1)	use v21 to test decoder	
00003094	E310 5018 0014		00000018	2049+	LGF	R1, V2ADDR	load v2 source	
0000309A	E761 0000 0806		00000000	2050+	VL	v22, 0(R1)	use v22 to test decoder	
000030A0	E310 501C 0014		0000001C	2051+	LGF	R1, V3ADDR	load v3 source	
000030A6	E771 0000 0806		00000000	2052+	VL	v23, 0(R1)	use v23 to test decoder	
000030AC	E756 7007 0E72			2053+	VERIM	V21, V22, V23, 7, 0	test instruction	
000030B2	E750 5030 080E		00003070	2054+	VST	V21, V1043	save v1 output	
000030B8	07FB			2055+	BR	R11	return	
000030BC				2056+RE43	DC	0F	xl16 expected result	
000030BC				2057+	DROP	R5		
000030BC	00800181 06860787			2058	DC	XL16' 0080018106860787 088809890E8E0F8F'	result t	
000030C4	08880989 0E8E0F8F							
000030CC	00010203 04050607			2059	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
000030D4	08090A0B 0C0D0E0F							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000030DC	00010203 04050607			2060	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
000030E4	08090A0B 0C0D0E0F							
000030EC	C3C3C3C3 C3C3C3C3			2061	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
000030F4	C3C3C3C3 C3C3C3C3							
				2062				
00003100				2063	VRI_D	VERIM, 255, 0	255->1 right	
00003100		00003100		2064+	DS	OFD		
00003100	00003148			2065+	USING	*, R5	base for test data and test routine	
00003104	002C			2066+T44	DC	A(X44)	address of test routine	
00003106	00			2067+	DC	H' 44'	test number	
00003107	FF			2068+	DC	X' 00'		
00003108	00			2069+	DC	HL1' 255'	i4 field	
00003109	E5C5D9C9 D4404040			2070+	DC	HL1' 0'	m5 field	
00003114	0000318C			2071+	DC	CL8' VERIM	instruction name	
00003118	0000319C			2072+	DC	A(RE44+16)	address of v1 source	
0000311C	000031AC			2073+	DC	A(RE44+32)	address of v2 source	
00003120	00000010			2074+	DC	A(RE44+48)	address of v3 source	
00003124	0000317C			2075+	DC	A(16)	result length	
00003128	00000000 00000000			2076+REA44	DC	A(RE44)	result address	
00003130	00000000 00000000			2077+	DS	FD	gap	
00003138	00000000 00000000			2078+V1044	DS	XL16	V1 output	
00003140	00000000 00000000							
				2079+	DS	FD	gap	
00003148				2080+*				
00003148	E310 5014 0014		00000014	2081+X44	DS	OF		
0000314E	E751 0000 0806		00000000	2082+	LGF	R1, V1ADDR	load v1 source	
00003154	E310 5018 0014		00000018	2083+	VL	v21, 0(R1)	use v21 to test decoder	
0000315A	E761 0000 0806		00000000	2084+	LGF	R1, V2ADDR	load v2 source	
00003160	E310 501C 0014		0000001C	2085+	VL	v22, 0(R1)	use v22 to test decoder	
00003166	E771 0000 0806		00000000	2086+	LGF	R1, V3ADDR	load v3 source	
0000316C	E756 70FF 0E72			2087+	VL	v23, 0(R1)	use v23 to test decoder	
00003172	E750 5030 080E		00003130	2088+	VERIM	V21, V22, V23, 255, 0	test instruction	
00003178	07FB			2089+	VST	V21, V1044	save v1 output	
0000317C				2090+	BR	R11	return	
0000317C				2091+RE44	DC	OF	xl16 expected result	
0000317C	00800181 06860787			2092+	DROP	R5		
00003184	08880989 0E8E0F8F			2093	DC	XL16' 0080018106860787 088809890E8E0F8F'	result t	
0000318C	00010203 04050607			2094	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003194	08090A0B 0C0D0E0F							
0000319C	00010203 04050607			2095	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
000031A4	08090A0B 0C0D0E0F							
000031AC	C3C3C3C3 C3C3C3C3			2096	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
000031B4	C3C3C3C3 C3C3C3C3							
				2097				
000031C0				2098	VRI_D	VERIM, 254, 0	254->2 right	
000031C0		000031C0		2099+	DS	OFD		
000031C0	00003208			2100+	USING	*, R5	base for test data and test routine	
000031C4	002D			2101+T45	DC	A(X45)	address of test routine	
000031C6	00			2102+	DC	H' 45'	test number	
000031C7	FE			2103+	DC	X' 00'		
000031C8	00			2104+	DC	HL1' 254'	i4 field	
000031C9	E5C5D9C9 D4404040			2105+	DC	HL1' 0'	m5 field	
000031D4	0000324C			2106+	DC	CL8' VERIM	instruction name	
000031D8	0000325C			2107+	DC	A(RE45+16)	address of v1 source	
				2108+	DC	A(RE45+32)	address of v2 source	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000031DC	0000326C			2109+	DC	A(RE45+48)	address of v3 source
000031E0	00000010			2110+	DC	A(16)	result length
000031E4	0000323C			2111+REA45	DC	A(RE45)	result address
000031E8	00000000 00000000			2112+	DS	FD	gap
000031F0	00000000 00000000			2113+V1045	DS	XL16	V1 output
000031F8	00000000 00000000						
00003200	00000000 00000000			2114+	DS	FD	gap
				2115+*			
00003208				2116+X45	DS	OF	
00003208	E310 5014 0014		00000014	2117+	LGF	R1, V1ADDR	load v1 source
0000320E	E751 0000 0806		00000000	2118+	VL	v21, 0(R1)	use v21 to test decoder
00003214	E310 5018 0014		00000018	2119+	LGF	R1, V2ADDR	load v2 source
0000321A	E761 0000 0806		00000000	2120+	VL	v22, 0(R1)	use v22 to test decoder
00003220	E310 501C 0014		0000001C	2121+	LGF	R1, V3ADDR	load v3 source
00003226	E771 0000 0806		00000000	2122+	VL	v23, 0(R1)	use v23 to test decoder
0000322C	E756 70FE 0E72			2123+	VERIM	V21, V22, V23, 254, 0	test instruction
00003232	E750 5030 080E		000031F0	2124+	VST	V21, V1045	save v1 output
00003238	07FB			2125+	BR	R11	return
0000323C				2126+RE45	DC	OF	xl16 expected result
0000323C				2127+	DROP	R5	
0000323C	004080C0 054585C5			2128	DC	XL16' 004080C0054585C5 0A4A8ACA0F4F8FCF'	result t
00003244	0A4A8ACA 0F4F8FCF						
0000324C	00010203 04050607			2129	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003254	08090A0B 0C0D0E0F						
0000325C	00010203 04050607			2130	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003264	08090A0B 0C0D0E0F						
0000326C	C3C3C3C3 C3C3C3C3			2131	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003274	C3C3C3C3 C3C3C3C3						
				2132			
00003280				2133	VRI_D	VERIM, 250, 0	250->6 right
00003280		00003280		2134+	DS	OFD	
00003280	000032C8			2135+	USING	*, R5	base for test data and test routine
00003284	002E			2136+T46	DC	A(X46)	address of test routine
00003286	00			2137+	DC	H' 46'	test number
00003287	FA			2138+	DC	X' 00'	
00003288	00			2139+	DC	HL1' 250'	i4 field
00003288	00			2140+	DC	HL1' 0'	m5 field
00003289	E5C5D9C9 D4404040			2141+	DC	CL8' VERIM	instruction name
00003294	0000330C			2142+	DC	A(RE46+16)	address of v1 source
00003298	0000331C			2143+	DC	A(RE46+32)	address of v2 source
0000329C	0000332C			2144+	DC	A(RE46+48)	address of v3 source
000032A0	00000010			2145+	DC	A(16)	result length
000032A4	000032FC			2146+REA46	DC	A(RE46)	result address
000032A8	00000000 00000000			2147+	DS	FD	gap
000032B0	00000000 00000000			2148+V1046	DS	XL16	V1 output
000032B8	00000000 00000000						
000032C0	00000000 00000000			2149+	DS	FD	gap
				2150+*			
000032C8				2151+X46	DS	OF	
000032C8	E310 5014 0014		00000014	2152+	LGF	R1, V1ADDR	load v1 source
000032CE	E751 0000 0806		00000000	2153+	VL	v21, 0(R1)	use v21 to test decoder
000032D4	E310 5018 0014		00000018	2154+	LGF	R1, V2ADDR	load v2 source
000032DA	E761 0000 0806		00000000	2155+	VL	v22, 0(R1)	use v22 to test decoder
000032E0	E310 501C 0014		0000001C	2156+	LGF	R1, V3ADDR	load v3 source
000032E6	E771 0000 0806		00000000	2157+	VL	v23, 0(R1)	use v23 to test decoder
000032EC	E756 70FA 0E72			2158+	VERIM	V21, V22, V23, 250, 0	test instruction

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000032F2	E750 5030 080E		000032B0	2159+	VST	V21, V1046	save v1 output
000032F8	07FB			2160+	BR	R11	return
000032FC				2161+RE46	DC	0F	xl16 expected result
000032FC				2162+	DROP	R5	
000032FC	00000000 04040404			2163	DC	XL16' 0000000004040404 080808080C0C0C0C'	result t
00003304	08080808 0C0C0C0C						
0000330C	00010203 04050607			2164	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003314	08090A0B 0C0D0E0F						
0000331C	00010203 04050607			2165	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003324	08090A0B 0C0D0E0F						
0000332C	C3C3C3C3 C3C3C3C3			2166	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003334	C3C3C3C3 C3C3C3C3						
				2167			
				2168	VRI_D	VERIM, 248, 0	248-8 right
00003340				2169+	DS	0FD	
00003340		00003340		2170+	USING	*, R5	base for test data and test routine
00003340	00003388			2171+T47	DC	A(X47)	address of test routine
00003344	002F			2172+	DC	H' 47'	test number
00003346	00			2173+	DC	X' 00'	
00003347	F8			2174+	DC	HL1' 248'	i4 field
00003348	00			2175+	DC	HL1' 0'	m5 field
00003349	E5C5D9C9 D4404040			2176+	DC	CL8' VERIM	instruction name
00003354	000033CC			2177+	DC	A(RE47+16)	address of v1 source
00003358	000033DC			2178+	DC	A(RE47+32)	address of v2 source
0000335C	000033EC			2179+	DC	A(RE47+48)	address of v3 source
00003360	00000010			2180+	DC	A(16)	result length
00003364	000033BC			2181+REA47	DC	A(RE47)	result address
00003368	00000000 00000000			2182+	DS	FD	gap
00003370	00000000 00000000			2183+V1047	DS	XL16	V1 output
00003378	00000000 00000000						
00003380	00000000 00000000			2184+	DS	FD	gap
				2185+*			
00003388				2186+X47	DS	0F	
00003388	E310 5014 0014		00000014	2187+	LGF	R1, V1ADDR	load v1 source
0000338E	E751 0000 0806		00000000	2188+	VL	v21, 0(R1)	use v21 to test decoder
00003394	E310 5018 0014		00000018	2189+	LGF	R1, V2ADDR	load v2 source
0000339A	E761 0000 0806		00000000	2190+	VL	v22, 0(R1)	use v22 to test decoder
000033A0	E310 501C 0014		0000001C	2191+	LGF	R1, V3ADDR	load v3 source
000033A6	E771 0000 0806		00000000	2192+	VL	v23, 0(R1)	use v23 to test decoder
000033AC	E756 70F8 0E72			2193+	VERIM	V21, V22, V23, 248, 0	test instruction
000033B2	E750 5030 080E		00003370	2194+	VST	V21, V1047	save v1 output
000033B8	07FB			2195+	BR	R11	return
000033BC				2196+RE47	DC	0F	xl16 expected result
000033BC				2197+	DROP	R5	
000033BC	00010203 04050607			2198	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	result t
000033C4	08090A0B 0C0D0E0F						
000033CC	00010203 04050607			2199	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
000033D4	08090A0B 0C0D0E0F						
000033DC	00010203 04050607			2200	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000033E4	08090A0B 0C0D0E0F						
000033EC	C3C3C3C3 C3C3C3C3			2201	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000033F4	C3C3C3C3 C3C3C3C3						
				2202			

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2204 *Halfword		
				2205	VRI_D VERIM, 0, 1	
00003400				2206+	DS OFD	
00003400		00003400		2207+	USING *, R5	base for test data and test routine
00003400	00003448			2208+T48	DC A(X48)	address of test routine
00003404	0030			2209+	DC H' 48'	test number
00003406	00			2210+	DC X' 00'	
00003407	00			2211+	DC HL1' 0'	i4 field
00003408	01			2212+	DC HL1' 1'	m5 field
00003409	E5C5D9C9 D4404040			2213+	DC CL8' VERIM	instruction name
00003414	0000348C			2214+	DC A(RE48+16)	address of v1 source
00003418	0000349C			2215+	DC A(RE48+32)	address of v2 source
0000341C	000034AC			2216+	DC A(RE48+48)	address of v3 source
00003420	00000010			2217+	DC A(16)	result length
00003424	0000347C			2218+REA48	DC A(RE48)	result address
00003428	00000000 00000000			2219+	DS FD	gap
00003430	00000000 00000000			2220+V1048	DS XL16	V1 output
00003438	00000000 00000000					
00003440	00000000 00000000			2221+	DS FD	gap
				2222+*		
00003448				2223+X48	DS OF	
00003448	E310 5014 0014		00000014	2224+	LGF R1, V1ADDR	load v1 source
0000344E	E751 0000 0806		00000000	2225+	VL v21, 0(R1)	use v21 to test decoder
00003454	E310 5018 0014		00000018	2226+	LGF R1, V2ADDR	load v2 source
0000345A	E761 0000 0806		00000000	2227+	VL v22, 0(R1)	use v22 to test decoder
00003460	E310 501C 0014		0000001C	2228+	LGF R1, V3ADDR	load v3 source
00003466	E771 0000 0806		00000000	2229+	VL v23, 0(R1)	use v23 to test decoder
0000346C	E756 7000 1E72			2230+	VERIM V21, V22, V23, 0, 1	test instruction
00003472	E750 5030 080E		00003430	2231+	VST V21, V1048	save v1 output
00003478	07FB			2232+	BR R11	return
0000347C				2233+RE48	DC OF	xl16 expected result
0000347C				2234+	DROP R5	
0000347C	00010203 04050607			2235	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	result t
00003484	08090A0B 0C0D0E0F					
0000348C	00010203 04050607			2236	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003494	08090A0B 0C0D0E0F					
0000349C	00010203 04050607			2237	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000034A4	08090A0B 0C0D0E0F					
000034AC	00000000 00000000			2238	DC XL16' 0000000000000000 0000000000000000'	v3
000034B4	00000000 00000000					
				2239		
				2240	VRI_D VERIM, 1, 1	
000034C0				2241+	DS OFD	
000034C0		000034C0		2242+	USING *, R5	base for test data and test routine
000034C0	00003508			2243+T49	DC A(X49)	address of test routine
000034C4	0031			2244+	DC H' 49'	test number
000034C6	00			2245+	DC X' 00'	
000034C7	01			2246+	DC HL1' 1'	i4 field
000034C8	01			2247+	DC HL1' 1'	m5 field
000034C9	E5C5D9C9 D4404040			2248+	DC CL8' VERIM	instruction name
000034D4	0000354C			2249+	DC A(RE49+16)	address of v1 source
000034D8	0000355C			2250+	DC A(RE49+32)	address of v2 source
000034DC	0000356C			2251+	DC A(RE49+48)	address of v3 source
000034E0	00000010			2252+	DC A(16)	result length
000034E4	0000353C			2253+REA49	DC A(RE49)	result address
000034E8	00000000 00000000			2254+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000034F0	00000000 00000000			2255+V1049	DS	XL16	V1 output
000034F8	00000000 00000000						
00003500	00000000 00000000			2256+ 2257+*	DS	FD	gap
00003508				2258+X49	DS	OF	
00003508	E310 5014 0014		00000014	2259+	LGF	R1, V1ADDR	load v1 source
0000350E	E751 0000 0806		00000000	2260+	VL	v21, 0(R1)	use v21 to test decoder
00003514	E310 5018 0014		00000018	2261+	LGF	R1, V2ADDR	load v2 source
0000351A	E761 0000 0806		00000000	2262+	VL	v22, 0(R1)	use v22 to test decoder
00003520	E310 501C 0014		0000001C	2263+	LGF	R1, V3ADDR	load v3 source
00003526	E771 0000 0806		00000000	2264+	VL	v23, 0(R1)	use v23 to test decoder
0000352C	E756 7001 1E72			2265+	VERIM	V21, V22, V23, 1, 1	test instruction
00003532	E750 5030 080E		000034F0	2266+	VST	V21, V1049	save v1 output
00003538	07FB			2267+	BR	R11	return
0000353C				2268+RE49	DC	OF	xl16 expected result
0000353C				2269+	DROP	R5	
0000353C	00020002 04060406			2270	DC	XL16' 0002000204060406 080A080A0C0E0C0E'	result t
00003544	080A080A 0C0E0C0E						
0000354C	00010203 04050607			2271	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003554	08090A0B 0C0D0E0F						
0000355C	00010203 04050607			2272	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003564	08090A0B 0C0D0E0F						
0000356C	C3C3C3C3 C3C3C3C3			2273	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003574	C3C3C3C3 C3C3C3C3						
				2274			
				2275	VRI_D	VERIM, 2, 1	
00003580				2276+	DS	OFD	
00003580		00003580		2277+	USING	*, R5	base for test data and test routine
00003580	000035C8			2278+T50	DC	A(X50)	address of test routine
00003584	0032			2279+	DC	H' 50'	test number
00003586	00			2280+	DC	X' 00'	
00003587	02			2281+	DC	HL1' 2'	i4 field
00003588	01			2282+	DC	HL1' 1'	m5 field
00003589	E5C5D9C9 D4404040			2283+	DC	CL8' VERIM	instruction name
00003594	0000360C			2284+	DC	A(RE50+16)	address of v1 source
00003598	0000361C			2285+	DC	A(RE50+32)	address of v2 source
0000359C	0000362C			2286+	DC	A(RE50+48)	address of v3 source
000035A0	00000010			2287+	DC	A(16)	result length
000035A4	000035FC			2288+REA50	DC	A(RE50)	result address
000035A8	00000000 00000000			2289+	DS	FD	gap
000035B0	00000000 00000000			2290+V1050	DS	XL16	V1 output
000035B8	00000000 00000000						
000035C0	00000000 00000000			2291+ 2292+*	DS	FD	gap
000035C8				2293+X50	DS	OF	
000035C8	E310 5014 0014		00000014	2294+	LGF	R1, V1ADDR	load v1 source
000035CE	E751 0000 0806		00000000	2295+	VL	v21, 0(R1)	use v21 to test decoder
000035D4	E310 5018 0014		00000018	2296+	LGF	R1, V2ADDR	load v2 source
000035DA	E761 0000 0806		00000000	2297+	VL	v22, 0(R1)	use v22 to test decoder
000035E0	E310 501C 0014		0000001C	2298+	LGF	R1, V3ADDR	load v3 source
000035E6	E771 0000 0806		00000000	2299+	VL	v23, 0(R1)	use v23 to test decoder
000035EC	E756 7002 1E72			2300+	VERIM	V21, V22, V23, 2, 1	test instruction
000035F2	E750 5030 080E		000035B0	2301+	VST	V21, V1050	save v1 output
000035F8	07FB			2302+	BR	R11	return
000035FC				2303+RE50	DC	OF	xl16 expected result
000035FC				2304+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
000035FC	00000000	04040404		2305	DC	XL16' 0000000004040404 080808080C0C0C0C'	result
00003604	08080808	0C0C0C0C					
0000360C	00010203	04050607		2306	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003614	08090A0B	0C0D0E0F					
0000361C	00010203	04050607		2307	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003624	08090A0B	0C0D0E0F					
0000362C	C3C3C3C3	C3C3C3C3		2308	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003634	C3C3C3C3	C3C3C3C3					
				2309			
00003640				2310	VRI_D	VERIM 5, 1	
00003640			00003640	2311+	DS	OFD	
00003640	00003688			2312+	USING	*, R5	base for test data and test routine
00003644	0033			2313+T51	DC	A(X51)	address of test routine
00003646	00			2314+	DC	H' 51'	test number
00003647	05			2315+	DC	X' 00'	
00003648	01			2316+	DC	HL1' 5'	i4 field
00003649	E5C5D9C9	D4404040		2317+	DC	HL1' 1'	m5 field
00003654	000036CC			2318+	DC	CL8' VERIM	instruction name
00003658	000036DC			2319+	DC	A(RE51+16)	address of v1 source
0000365C	000036EC			2320+	DC	A(RE51+32)	address of v2 source
00003660	00000010			2321+	DC	A(RE51+48)	address of v3 source
00003664	000036BC			2322+	DC	A(16)	result length
00003668	00000000	00000000		2323+REA51	DC	A(RE51)	result address
00003670	00000000	00000000		2324+	DS	FD	gap
00003678	00000000	00000000		2325+V1051	DS	XL16	V1 output
00003680	00000000	00000000					
				2326+	DS	FD	gap
00003688				2327+*			
00003688	E310 5014 0014		00000014	2328+X51	DS	OF	
0000368E	E751 0000 0806		00000000	2329+	LGF	R1, V1ADDR	load v1 source
00003694	E310 5018 0014		00000018	2330+	VL	v21, 0(R1)	use v21 to test decoder
0000369A	E761 0000 0806		00000000	2331+	LGF	R1, V2ADDR	load v2 source
000036A0	E310 501C 0014		0000001C	2332+	VL	v22, 0(R1)	use v22 to test decoder
000036A6	E771 0000 0806		00000000	2333+	LGF	R1, V3ADDR	load v3 source
000036AC	E756 7005 1E72			2334+	VL	v23, 0(R1)	use v23 to test decoder
000036B2	E750 5030 080E		00003670	2335+	VERIM	V21, V22, V23, 5, 1	test instruction
000036B8	07FB			2336+	VST	V21, V1051	save v1 output
000036BC				2337+	BR	R11	return
000036BC				2338+RE51	DC	OF	xl16 expected result
000036BC				2339+	DROP	R5	
000036BC	00004040	8484C4C4		2340	DC	XL16' 000040408484C4C4 090949498D8DCDCD'	result
000036C4	09094949	8D8DCDCD					
000036CC	00010203	04050607		2341	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
000036D4	08090A0B	0C0D0E0F					
000036DC	00010203	04050607		2342	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000036E4	08090A0B	0C0D0E0F					
000036EC	C3C3C3C3	C3C3C3C3		2343	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000036F4	C3C3C3C3	C3C3C3C3					
				2344			
00003700				2345	VRI_D	VERIM 7, 1	
00003700			00003700	2346+	DS	OFD	
00003700	00003748			2347+	USING	*, R5	base for test data and test routine
00003704	0034			2348+T52	DC	A(X52)	address of test routine
00003706	00			2349+	DC	H' 52'	test number
00003707	07			2350+	DC	X' 00'	
				2351+	DC	HL1' 7'	i4 field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003708	01			2352+	DC	HL1' 1'	m5 field
00003709	E5C5D9C9 D4404040			2353+	DC	CL8' VERIM	instruction name
00003714	0000378C			2354+	DC	A(RE52+16)	address of v1 source
00003718	0000379C			2355+	DC	A(RE52+32)	address of v2 source
0000371C	000037AC			2356+	DC	A(RE52+48)	address of v3 source
00003720	00000010			2357+	DC	A(16)	result length
00003724	0000377C			2358+REA52	DC	A(RE52)	result address
00003728	00000000 00000000			2359+	DS	FD	gap
00003730	00000000 00000000			2360+V1052	DS	XL16	V1 output
00003738	00000000 00000000						
00003740	00000000 00000000			2361+	DS	FD	gap
				2362+*			
00003748				2363+X52	DS	0F	
00003748	E310 5014 0014		00000014	2364+	LGF	R1, V1ADDR	load v1 source
0000374E	E751 0000 0806		00000000	2365+	VL	v21, 0(R1)	use v21 to test decoder
00003754	E310 5018 0014		00000018	2366+	LGF	R1, V2ADDR	load v2 source
0000375A	E761 0000 0806		00000000	2367+	VL	v22, 0(R1)	use v22 to test decoder
00003760	E310 501C 0014		0000001C	2368+	LGF	R1, V3ADDR	load v3 source
00003766	E771 0000 0806		00000000	2369+	VL	v23, 0(R1)	use v23 to test decoder
0000376C	E756 7007 1E72			2370+	VERIM	V21, V22, V23, 7, 1	test instruction
00003772	E750 5030 080E		00003730	2371+	VST	V21, V1052	save v1 output
00003778	07FB			2372+	BR	R11	return
0000377C				2373+RE52	DC	0F	xl16 expected result
0000377C				2374+	DROP	R5	
0000377C	00800181 06860787			2375	DC	XL16' 0080018106860787 088809890E8E0F8F'	result t
00003784	08880989 0E8E0F8F						
0000378C	00010203 04050607			2376	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003794	08090A0B 0C0D0E0F						
0000379C	00010203 04050607			2377	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000037A4	08090A0B 0C0D0E0F						
000037AC	C3C3C3C3 C3C3C3C3			2378	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000037B4	C3C3C3C3 C3C3C3C3						
				2379			
000037C0				2380	VRI_D	VERIM, 255, 1	255->1 right
000037C0		000037C0		2381+	DS	0FD	
000037C0	00003808			2382+	USING	*, R5	base for test data and test routine
000037C4	0035			2383+T53	DC	A(X53)	address of test routine
000037C6	00			2384+	DC	H' 53'	test number
000037C7	FF			2385+	DC	X' 00'	
000037C8	01			2386+	DC	HL1' 255'	i4 field
000037C9	E5C5D9C9 D4404040			2387+	DC	HL1' 1'	m5 field
000037D4	0000384C			2388+	DC	CL8' VERIM	instruction name
000037D8	0000385C			2389+	DC	A(RE53+16)	address of v1 source
000037DC	0000386C			2390+	DC	A(RE53+32)	address of v2 source
000037E0	00000010			2391+	DC	A(RE53+48)	address of v3 source
000037E4	0000383C			2392+	DC	A(16)	result length
000037E8	00000000 00000000			2393+REA53	DC	A(RE53)	result address
000037F0	00000000 00000000			2394+	DS	FD	gap
000037F8	00000000 00000000			2395+V1053	DS	XL16	V1 output
00003800	00000000 00000000			2396+	DS	FD	gap
				2397+*			
00003808				2398+X53	DS	0F	
00003808	E310 5014 0014		00000014	2399+	LGF	R1, V1ADDR	load v1 source
0000380E	E751 0000 0806		00000000	2400+	VL	v21, 0(R1)	use v21 to test decoder
00003814	E310 5018 0014		00000018	2401+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
0000381A	E761 0000 0806		00000000	2402+	VL	v22, 0(R1)	use v22 to test decoder	
00003820	E310 501C 0014		0000001C	2403+	LGF	R1, V3ADDR	load v3 source	
00003826	E771 0000 0806		00000000	2404+	VL	v23, 0(R1)	use v23 to test decoder	
0000382C	E756 70FF 1E72			2405+	VERIM	V21, V22, V23, 255, 1	test instruction	
00003832	E750 5030 080E		000037F0	2406+	VST	V21, V1053	save v1 output	
00003838	07FB			2407+	BR	R11	return	
0000383C				2408+RE53	DC	0F	xl16 expected result	
0000383C				2409+	DROP	R5		
0000383C	80008101 86068707			2410	DC	XL16' 8000810186068707 880889098E0E8F0F'	result t	
00003844	88088909 8E0E8F0F							
0000384C	00010203 04050607			2411	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003854	08090A0B 0C0D0E0F							
0000385C	00010203 04050607			2412	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00003864	08090A0B 0C0D0E0F							
0000386C	C3C3C3C3 C3C3C3C3			2413	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00003874	C3C3C3C3 C3C3C3C3							
				2414				
00003880				2415	VRI_D	VERIM, 254, 1	254->2 right	
00003880		00003880		2416+	DS	0FD		
00003880	000038C8			2417+	USING	*, R5	base for test data and test routine	
00003884	0036			2418+T54	DC	A(X54)	address of test routine	
00003886	00			2419+	DC	H' 54'	test number	
00003887	FE			2420+	DC	X' 00'		
00003888	01			2421+	DC	HL1' 254'	i4 field	
00003889	E5C5D9C9 D4404040			2422+	DC	HL1' 1'	m5 field	
00003894	0000390C			2423+	DC	CL8' VERIM	instruction name	
00003898	0000391C			2424+	DC	A(RE54+16)	address of v1 source	
0000389C	0000392C			2425+	DC	A(RE54+32)	address of v2 source	
000038A0	00000010			2426+	DC	A(RE54+48)	address of v3 source	
000038A4	000038FC			2427+	DC	A(16)	result length	
000038A8	00000000 00000000			2428+REA54	DC	A(RE54)	result address	
000038B0	00000000 00000000			2429+	DS	FD	gap	
000038B8	00000000 00000000			2430+V1054	DS	XL16	V1 output	
000038C0	00000000 00000000							
				2431+	DS	FD	gap	
000038C8				2432+*				
000038C8	E310 5014 0014		00000014	2433+X54	DS	0F		
000038CE	E751 0000 0806		00000000	2434+	LGF	R1, V1ADDR	load v1 source	
000038D4	E310 5018 0014		00000018	2435+	VL	v21, 0(R1)	use v21 to test decoder	
000038DA	E761 0000 0806		00000000	2436+	LGF	R1, V2ADDR	load v2 source	
000038E0	E310 501C 0014		0000001C	2437+	VL	v22, 0(R1)	use v22 to test decoder	
000038E6	E771 0000 0806		00000000	2438+	LGF	R1, V3ADDR	load v3 source	
000038EC	E756 70FE 1E72			2439+	VL	v23, 0(R1)	use v23 to test decoder	
000038F2	E750 5030 080E		000038B0	2440+	VERIM	V21, V22, V23, 254, 1	test instruction	
000038F8	07FB			2441+	VST	V21, V1054	save v1 output	
000038FC				2442+	BR	R11	return	
000038FC				2443+RE54	DC	0F	xl16 expected result	
000038FC				2444+	DROP	R5		
000038FC	4000C080 4505C585			2445	DC	XL16' 4000C0804505C585 4A0ACA8A4F0FCF8F'	result t	
00003904	4A0ACA8A 4F0FCF8F							
0000390C	00010203 04050607			2446	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003914	08090A0B 0C0D0E0F							
0000391C	00010203 04050607			2447	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00003924	08090A0B 0C0D0E0F							
0000392C	C3C3C3C3 C3C3C3C3			2448	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00003934	C3C3C3C3 C3C3C3C3							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2449		
				2450	VRI_D VERIM, 250, 1	250->6 right
00003940				2451+	DS OFD	
00003940		00003940		2452+	USING *, R5	base for test data and test routine
00003940	00003988			2453+T55	DC A(X55)	address of test routine
00003944	0037			2454+	DC H' 55'	test number
00003946	00			2455+	DC X' 00'	
00003947	FA			2456+	DC HL1' 250'	i4 field
00003948	01			2457+	DC HL1' 1'	m5 field
00003949	E5C5D9C9 D4404040			2458+	DC CL8' VERIM	instruction name
00003954	000039CC			2459+	DC A(RE55+16)	address of v1 source
00003958	000039DC			2460+	DC A(RE55+32)	address of v2 source
0000395C	000039EC			2461+	DC A(RE55+48)	address of v3 source
00003960	00000010			2462+	DC A(16)	result length
00003964	000039BC			2463+REA55	DC A(RE55)	result address
00003968	00000000 00000000			2464+	DS FD	gap
00003970	00000000 00000000			2465+V1055	DS XL16	V1 output
00003978	00000000 00000000					
00003980	00000000 00000000			2466+	DS FD	gap
				2467+*		
00003988				2468+X55	DS OF	
00003988	E310 5014 0014		00000014	2469+	LGF R1, V1ADDR	load v1 source
0000398E	E751 0000 0806		00000000	2470+	VL v21, 0(R1)	use v21 to test decoder
00003994	E310 5018 0014		00000018	2471+	LGF R1, V2ADDR	load v2 source
0000399A	E761 0000 0806		00000000	2472+	VL v22, 0(R1)	use v22 to test decoder
000039A0	E310 501C 0014		0000001C	2473+	LGF R1, V3ADDR	load v3 source
000039A6	E771 0000 0806		00000000	2474+	VL v23, 0(R1)	use v23 to test decoder
000039AC	E756 70FA 1E72			2475+	VERIM V21, V22, V23, 250, 1	test instruction
000039B2	E750 5030 080E		00003970	2476+	VST V21, V1055	save v1 output
000039B8	07FB			2477+	BR R11	return
000039BC				2478+RE55	DC OF	xl16 expected result
000039BC				2479+	DROP R5	
000039BC	00000000 04040404			2480	DC XL16' 0000000004040404 080808080C0C0C0C'	result t
000039C4	08080808 0C0C0C0C					
000039CC	00010203 04050607			2481	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
000039D4	08090A0B 0C0D0E0F					
000039DC	00010203 04050607			2482	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000039E4	08090A0B 0C0D0E0F					
000039EC	C3C3C3C3 C3C3C3C3			2483	DC XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000039F4	C3C3C3C3 C3C3C3C3					
				2484		
				2485	VRI_D VERIM, 248, 1	248- 8 right
00003A00				2486+	DS OFD	
00003A00		00003A00		2487+	USING *, R5	base for test data and test routine
00003A00	00003A48			2488+T56	DC A(X56)	address of test routine
00003A04	0038			2489+	DC H' 56'	test number
00003A06	00			2490+	DC X' 00'	
00003A07	F8			2491+	DC HL1' 248'	i4 field
00003A08	01			2492+	DC HL1' 1'	m5 field
00003A09	E5C5D9C9 D4404040			2493+	DC CL8' VERIM	instruction name
00003A14	00003A8C			2494+	DC A(RE56+16)	address of v1 source
00003A18	00003A9C			2495+	DC A(RE56+32)	address of v2 source
00003A1C	00003AAC			2496+	DC A(RE56+48)	address of v3 source
00003A20	00000010			2497+	DC A(16)	result length
00003A24	00003A7C			2498+REA56	DC A(RE56)	result address
00003A28	00000000 00000000			2499+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
				2520 *Word			
				2521	VRI_D VERIM, 0, 2		
00003AC0				2522+	DS OFD		
00003AC0		00003AC0		2523+	USING *, R5	base for test data and test routine	
00003AC0	00003B08			2524+T57	DC A(X57)	address of test routine	
00003AC4	0039			2525+	DC H' 57'	test number	
00003AC6	00			2526+	DC X' 00'		
00003AC7	00			2527+	DC HL1' 0'	i4 field	
00003AC8	02			2528+	DC HL1' 2'	m5 field	
00003AC9	E5C5D9C9 D4404040			2529+	DC CL8' VERIM	instruction name	
00003AD4	00003B4C			2530+	DC A(RE57+16)	address of v1 source	
00003AD8	00003B5C			2531+	DC A(RE57+32)	address of v2 source	
00003ADC	00003B6C			2532+	DC A(RE57+48)	address of v3 source	
00003AE0	00000010			2533+	DC A(16)	result length	
00003AE4	00003B3C			2534+REA57	DC A(RE57)	result address	
00003AE8	00000000 00000000			2535+	DS FD	gap	
00003AF0	00000000 00000000			2536+V1057	DS XL16	V1 output	
00003AF8	00000000 00000000						
00003B00	00000000 00000000			2537+	DS FD	gap	
				2538+*			
00003B08				2539+X57	DS OF		
00003B08	E310 5014 0014		00000014	2540+	LGF R1, V1ADDR	load v1 source	
00003B0E	E751 0000 0806		00000000	2541+	VL v21, 0(R1)	use v21 to test decoder	
00003B14	E310 5018 0014		00000018	2542+	LGF R1, V2ADDR	load v2 source	
00003B1A	E761 0000 0806		00000000	2543+	VL v22, 0(R1)	use v22 to test decoder	
00003B20	E310 501C 0014		0000001C	2544+	LGF R1, V3ADDR	load v3 source	
00003B26	E771 0000 0806		00000000	2545+	VL v23, 0(R1)	use v23 to test decoder	
00003B2C	E756 7000 2E72			2546+	VERIM V21, V22, V23, 0, 2	test instruction	
00003B32	E750 5030 080E		00003AF0	2547+	VST V21, V1057	save v1 output	
00003B38	07FB			2548+	BR R11	return	
00003B3C				2549+RE57	DC OF	xl16 expected result	
00003B3C				2550+	DROP R5		
00003B3C	00010203 04050607			2551	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	result t	
00003B44	08090A0B 0C0D0E0F						
00003B4C	00010203 04050607			2552	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003B54	08090A0B 0C0D0E0F						
00003B5C	00010203 04050607			2553	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00003B64	08090A0B 0C0D0E0F						
00003B6C	00000000 00000000			2554	DC XL16' 0000000000000000 0000000000000000'	v3	
00003B74	00000000 00000000						
				2555			
				2556	VRI_D VERIM, 1, 2		
00003B80				2557+	DS OFD		
00003B80		00003B80		2558+	USING *, R5	base for test data and test routine	
00003B80	00003BC8			2559+T58	DC A(X58)	address of test routine	
00003B84	003A			2560+	DC H' 58'	test number	
00003B86	00			2561+	DC X' 00'		
00003B87	01			2562+	DC HL1' 1'	i4 field	
00003B88	02			2563+	DC HL1' 2'	m5 field	
00003B89	E5C5D9C9 D4404040			2564+	DC CL8' VERIM	instruction name	
00003B94	00003C0C			2565+	DC A(RE58+16)	address of v1 source	
00003B98	00003C1C			2566+	DC A(RE58+32)	address of v2 source	
00003B9C	00003C2C			2567+	DC A(RE58+48)	address of v3 source	
00003BA0	00000010			2568+	DC A(16)	result length	
00003BA4	00003BFC			2569+REA58	DC A(RE58)	result address	
00003BA8	00000000 00000000			2570+	DS FD	gap	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003BB0	00000000 00000000			2571+V1058	DS	XL16	V1 output
00003BB8	00000000 00000000						
00003BC0	00000000 00000000			2572+ 2573+*	DS	FD	gap
00003BC8				2574+X58	DS	OF	
00003BC8	E310 5014 0014		00000014	2575+	LGF	R1, V1ADDR	load v1 source
00003BCE	E751 0000 0806		00000000	2576+	VL	v21, 0(R1)	use v21 to test decoder
00003BD4	E310 5018 0014		00000018	2577+	LGF	R1, V2ADDR	load v2 source
00003BDA	E761 0000 0806		00000000	2578+	VL	v22, 0(R1)	use v22 to test decoder
00003BE0	E310 501C 0014		0000001C	2579+	LGF	R1, V3ADDR	load v3 source
00003BE6	E771 0000 0806		00000000	2580+	VL	v23, 0(R1)	use v23 to test decoder
00003BEC	E756 7001 2E72			2581+	VERIM	V21, V22, V23, 1, 2	test instruction
00003BF2	E750 5030 080E		00003BB0	2582+	VST	V21, V1058	save v1 output
00003BF8	07FB			2583+	BR	R11	return
00003BFC				2584+RE58	DC	OF	xl16 expected result
00003BFC				2585+	DROP	R5	
00003BFC	00020002 04060406			2586	DC	XL16' 0002000204060406 080A080A0C0E0C0E'	result t
00003C04	080A080A 0C0E0C0E						
00003C0C	00010203 04050607			2587	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003C14	08090A0B 0C0D0E0F						
00003C1C	00010203 04050607			2588	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003C24	08090A0B 0C0D0E0F						
00003C2C	C3C3C3C3 C3C3C3C3			2589	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003C34	C3C3C3C3 C3C3C3C3						
				2590			
				2591	VRI_D	VERIM, 2, 2	
00003C40				2592+	DS	OFD	
00003C40		00003C40		2593+	USING	*, R5	base for test data and test routine
00003C40	00003C88			2594+T59	DC	A(X59)	address of test routine
00003C44	003B			2595+	DC	H' 59'	test number
00003C46	00			2596+	DC	X' 00'	
00003C47	02			2597+	DC	HL1' 2'	i4 field
00003C48	02			2598+	DC	HL1' 2'	m5 field
00003C49	E5C5D9C9 D4404040			2599+	DC	CL8' VERIM	instruction name
00003C54	00003CCC			2600+	DC	A(RE59+16)	address of v1 source
00003C58	00003CDC			2601+	DC	A(RE59+32)	address of v2 source
00003C5C	00003CEC			2602+	DC	A(RE59+48)	address of v3 source
00003C60	00000010			2603+	DC	A(16)	result length
00003C64	00003CBC			2604+REA59	DC	A(RE59)	result address
00003C68	00000000 00000000			2605+	DS	FD	gap
00003C70	00000000 00000000			2606+V1059	DS	XL16	V1 output
00003C78	00000000 00000000						
00003C80	00000000 00000000			2607+ 2608+*	DS	FD	gap
00003C88				2609+X59	DS	OF	
00003C88	E310 5014 0014		00000014	2610+	LGF	R1, V1ADDR	load v1 source
00003C8E	E751 0000 0806		00000000	2611+	VL	v21, 0(R1)	use v21 to test decoder
00003C94	E310 5018 0014		00000018	2612+	LGF	R1, V2ADDR	load v2 source
00003C9A	E761 0000 0806		00000000	2613+	VL	v22, 0(R1)	use v22 to test decoder
00003CA0	E310 501C 0014		0000001C	2614+	LGF	R1, V3ADDR	load v3 source
00003CA6	E771 0000 0806		00000000	2615+	VL	v23, 0(R1)	use v23 to test decoder
00003CAC	E756 7002 2E72			2616+	VERIM	V21, V22, V23, 2, 2	test instruction
00003CB2	E750 5030 080E		00003C70	2617+	VST	V21, V1059	save v1 output
00003CB8	07FB			2618+	BR	R11	return
00003CBC				2619+RE59	DC	OF	xl16 expected result
00003CBC				2620+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003CBC	00000000 04040404			2621	DC	XL16' 0000000004040404 080808080C0C0C0C'	result
00003CC4	08080808 0C0C0C0C						
00003CCC	00010203 04050607			2622	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003CD4	08090A0B 0C0D0E0F						
00003CDC	00010203 04050607			2623	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003CE4	08090A0B 0C0D0E0F						
00003CEC	C3C3C3C3 C3C3C3C3			2624	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003CF4	C3C3C3C3 C3C3C3C3						
				2625			
00003D00				2626	VRI_D	VERIM 5, 2	
00003D00		00003D00		2627+	DS	OFD	
00003D00	00003D48			2628+	USING	*, R5	base for test data and test routine
00003D04	003C			2629+T60	DC	A(X60)	address of test routine
00003D06	00			2630+	DC	H' 60'	test number
00003D07	05			2631+	DC	X' 00'	
00003D08	02			2632+	DC	HL1' 5'	i4 field
00003D09	E5C5D9C9 D4404040			2633+	DC	HL1' 2'	m5 field
00003D14	00003D8C			2634+	DC	CL8' VERIM	instruction name
00003D18	00003D9C			2635+	DC	A(RE60+16)	address of v1 source
00003D1C	00003DAC			2636+	DC	A(RE60+32)	address of v2 source
00003D20	00000010			2637+	DC	A(RE60+48)	address of v3 source
00003D24	00003D7C			2638+	DC	A(16)	result length
00003D28	00000000 00000000			2639+REA60	DC	A(RE60)	result address
00003D30	00000000 00000000			2640+	DS	FD	gap
00003D38	00000000 00000000			2641+V1060	DS	XL16	V1 output
00003D40	00000000 00000000						
				2642+	DS	FD	gap
00003D48				2643+*			
00003D48	E310 5014 0014		00000014	2644+X60	DS	OF	
00003D4E	E751 0000 0806		00000000	2645+	LGF	R1, V1ADDR	load v1 source
00003D54	E310 5018 0014		00000018	2646+	VL	v21, 0(R1)	use v21 to test decoder
00003D5A	E761 0000 0806		00000000	2647+	LGF	R1, V2ADDR	load v2 source
00003D60	E310 501C 0014		0000001C	2648+	VL	v22, 0(R1)	use v22 to test decoder
00003D66	E771 0000 0806		00000000	2649+	LGF	R1, V3ADDR	load v3 source
00003D6C	E756 7005 2E72			2650+	VL	v23, 0(R1)	use v23 to test decoder
00003D72	E750 5030 080E		00003D30	2651+	VERIM	V21, V22, V23, 5, 2	test instruction
00003D78	07FB			2652+	VST	V21, V1060	save v1 output
00003D7C				2653+	BR	R11	return
00003D7C				2654+RE60	DC	OF	xl16 expected result
00003D7C	00004040 8484C4C4			2655+	DROP	R5	
00003D84	09094949 8D8DCDCD			2656	DC	XL16' 000040408484C4C4 090949498D8DCDCD'	result
00003D8C	00010203 04050607			2657	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003D94	08090A0B 0C0D0E0F						
00003D9C	00010203 04050607			2658	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003DA4	08090A0B 0C0D0E0F						
00003DAC	C3C3C3C3 C3C3C3C3			2659	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003DB4	C3C3C3C3 C3C3C3C3						
				2660			
00003DC0				2661	VRI_D	VERIM 7, 2	
00003DC0		00003DC0		2662+	DS	OFD	
00003DC0	00003E08			2663+	USING	*, R5	base for test data and test routine
00003DC4	003D			2664+T61	DC	A(X61)	address of test routine
00003DC6	00			2665+	DC	H' 61'	test number
00003DC7	07			2666+	DC	X' 00'	
				2667+	DC	HL1' 7'	i4 field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00003DC8	02			2668+	DC	HL1' 2'	m5 field
00003DC9	E5C5D9C9 D4404040			2669+	DC	CL8' VERIM	instruction name
00003DD4	00003E4C			2670+	DC	A(RE61+16)	address of v1 source
00003DD8	00003E5C			2671+	DC	A(RE61+32)	address of v2 source
00003DDC	00003E6C			2672+	DC	A(RE61+48)	address of v3 source
00003DE0	00000010			2673+	DC	A(16)	result length
00003DE4	00003E3C			2674+REA61	DC	A(RE61)	result address
00003DE8	00000000 00000000			2675+	DS	FD	gap
00003DF0	00000000 00000000			2676+V1061	DS	XL16	V1 output
00003DF8	00000000 00000000						
00003E00	00000000 00000000			2677+	DS	FD	gap
				2678+*			
00003E08				2679+X61	DS	0F	
00003E08	E310 5014 0014		00000014	2680+	LGF	R1, V1ADDR	load v1 source
00003E0E	E751 0000 0806		00000000	2681+	VL	v21, 0(R1)	use v21 to test decoder
00003E14	E310 5018 0014		00000018	2682+	LGF	R1, V2ADDR	load v2 source
00003E1A	E761 0000 0806		00000000	2683+	VL	v22, 0(R1)	use v22 to test decoder
00003E20	E310 501C 0014		0000001C	2684+	LGF	R1, V3ADDR	load v3 source
00003E26	E771 0000 0806		00000000	2685+	VL	v23, 0(R1)	use v23 to test decoder
00003E2C	E756 7007 2E72			2686+	VERIM	V21, V22, V23, 7, 2	test instruction
00003E32	E750 5030 080E		00003DF0	2687+	VST	V21, V1061	save v1 output
00003E38	07FB			2688+	BR	R11	return
00003E3C				2689+RE61	DC	0F	xl16 expected result
00003E3C				2690+	DROP	R5	
00003E3C	00810180 06870786			2691	DC	XL16' 0081018006870786 088909880E8F0F8E'	result t
00003E44	08890988 0E8F0F8E						
00003E4C	00010203 04050607			2692	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00003E54	08090A0B 0C0D0E0F						
00003E5C	00010203 04050607			2693	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00003E64	08090A0B 0C0D0E0F						
00003E6C	C3C3C3C3 C3C3C3C3			2694	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00003E74	C3C3C3C3 C3C3C3C3						
				2695			
				2696	VRI_D	VERIM, 255, 2	255->1 right
00003E80				2697+	DS	0FD	
00003E80		00003E80		2698+	USING	*, R5	base for test data and test routine
00003E80	00003EC8			2699+T62	DC	A(X62)	address of test routine
00003E84	003E			2700+	DC	H' 62'	test number
00003E86	00			2701+	DC	X' 00'	
00003E87	FF			2702+	DC	HL1' 255'	i4 field
00003E88	02			2703+	DC	HL1' 2'	m5 field
00003E89	E5C5D9C9 D4404040			2704+	DC	CL8' VERIM	instruction name
00003E94	00003F0C			2705+	DC	A(RE62+16)	address of v1 source
00003E98	00003F1C			2706+	DC	A(RE62+32)	address of v2 source
00003E9C	00003F2C			2707+	DC	A(RE62+48)	address of v3 source
00003EA0	00000010			2708+	DC	A(16)	result length
00003EA4	00003EFC			2709+REA62	DC	A(RE62)	result address
00003EA8	00000000 00000000			2710+	DS	FD	gap
00003EB0	00000000 00000000			2711+V1062	DS	XL16	V1 output
00003EB8	00000000 00000000						
00003EC0	00000000 00000000			2712+	DS	FD	gap
				2713+*			
00003EC8				2714+X62	DS	0F	
00003EC8	E310 5014 0014		00000014	2715+	LGF	R1, V1ADDR	load v1 source
00003ECE	E751 0000 0806		00000000	2716+	VL	v21, 0(R1)	use v21 to test decoder
00003ED4	E310 5018 0014		00000018	2717+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
00003EDA	E761 0000 0806		00000000	2718+	VL	v22, 0(R1)	use v22 to test decoder	
00003EE0	E310 501C 0014		0000001C	2719+	LGF	R1, V3ADDR	load v3 source	
00003EE6	E771 0000 0806		00000000	2720+	VL	v23, 0(R1)	use v23 to test decoder	
00003EEC	E756 70FF 2E72			2721+	VERIM	V21, V22, V23, 255, 2	test instruction	
00003EF2	E750 5030 080E		00003EB0	2722+	VST	V21, V1062	save v1 output	
00003EF8	07FB			2723+	BR	R11	return	
00003EFC				2724+RE62	DC	0F	xl16 expected result	
00003EFC				2725+	DROP	R5		
00003EFC	80008101 86068707			2726	DC	XL16' 8000810186068707 880889098E0E8F0F'	result t	
00003F04	88088909 8E0E8F0F							
00003F0C	00010203 04050607			2727	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003F14	08090A0B 0C0D0E0F							
00003F1C	00010203 04050607			2728	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00003F24	08090A0B 0C0D0E0F							
00003F2C	C3C3C3C3 C3C3C3C3			2729	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00003F34	C3C3C3C3 C3C3C3C3							
				2730				
00003F40				2731	VRI_D	VERIM, 254, 2	254->2 right	
00003F40		00003F40		2732+	DS	0FD		
00003F40	00003F88			2733+	USING	*, R5	base for test data and test routine	
00003F44	003F			2734+T63	DC	A(X63)	address of test routine	
00003F46	00			2735+	DC	H' 63'	test number	
00003F46	00			2736+	DC	X' 00'		
00003F47	FE			2737+	DC	HL1' 254'	i4 field	
00003F48	02			2738+	DC	HL1' 2'	m5 field	
00003F49	E5C5D9C9 D4404040			2739+	DC	CL8' VERIM	instruction name	
00003F54	00003FCC			2740+	DC	A(RE63+16)	address of v1 source	
00003F58	00003FDC			2741+	DC	A(RE63+32)	address of v2 source	
00003F5C	00003FEC			2742+	DC	A(RE63+48)	address of v3 source	
00003F60	00000010			2743+	DC	A(16)	result length	
00003F64	00003FBC			2744+REA63	DC	A(RE63)	result address	
00003F68	00000000 00000000			2745+	DS	FD	gap	
00003F70	00000000 00000000			2746+V1063	DS	XL16	V1 output	
00003F78	00000000 00000000							
00003F80	00000000 00000000			2747+	DS	FD	gap	
				2748+*				
00003F88				2749+X63	DS	0F		
00003F88	E310 5014 0014		00000014	2750+	LGF	R1, V1ADDR	load v1 source	
00003F8E	E751 0000 0806		00000000	2751+	VL	v21, 0(R1)	use v21 to test decoder	
00003F94	E310 5018 0014		00000018	2752+	LGF	R1, V2ADDR	load v2 source	
00003F9A	E761 0000 0806		00000000	2753+	VL	v22, 0(R1)	use v22 to test decoder	
00003FA0	E310 501C 0014		0000001C	2754+	LGF	R1, V3ADDR	load v3 source	
00003FA6	E771 0000 0806		00000000	2755+	VL	v23, 0(R1)	use v23 to test decoder	
00003FAC	E756 70FE 2E72			2756+	VERIM	V21, V22, V23, 254, 2	test instruction	
00003FB2	E750 5030 080E		00003F70	2757+	VST	V21, V1063	save v1 output	
00003FB8	07FB			2758+	BR	R11	return	
00003FBC				2759+RE63	DC	0F	xl16 expected result	
00003FBC				2760+	DROP	R5		
00003FBC	C0004080 C5054585			2761	DC	XL16' C0004080C5054585 CA0A4A8ACF0F4F8F'	result t	
00003FC4	CA0A4A8A CF0F4F8F							
00003FCC	00010203 04050607			2762	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00003FD4	08090A0B 0C0D0E0F							
00003FDC	00010203 04050607			2763	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00003FE4	08090A0B 0C0D0E0F							
00003FEC	C3C3C3C3 C3C3C3C3			2764	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00003FF4	C3C3C3C3 C3C3C3C3							

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2765		
				2766	VRI_D VERIM, 250, 2	250->6 right
00004000				2767+	DS OFD	
00004000		00004000		2768+	USING *, R5	base for test data and test routine
00004000	00004048			2769+T64	DC A(X64)	address of test routine
00004004	0040			2770+	DC H' 64'	test number
00004006	00			2771+	DC X' 00'	
00004007	FA			2772+	DC HL1' 250'	i4 field
00004008	02			2773+	DC HL1' 2'	m5 field
00004009	E5C5D9C9 D4404040			2774+	DC CL8' VERIM	instruction name
00004014	0000408C			2775+	DC A(RE64+16)	address of v1 source
00004018	0000409C			2776+	DC A(RE64+32)	address of v2 source
0000401C	000040AC			2777+	DC A(RE64+48)	address of v3 source
00004020	00000010			2778+	DC A(16)	result length
00004024	0000407C			2779+REA64	DC A(RE64)	result address
00004028	00000000 00000000			2780+	DS FD	gap
00004030	00000000 00000000			2781+V1064	DS XL16	V1 output
00004038	00000000 00000000					
00004040	00000000 00000000			2782+	DS FD	gap
				2783+*		
00004048				2784+X64	DS OF	
00004048	E310 5014 0014		00000014	2785+	LGF R1, V1ADDR	load v1 source
0000404E	E751 0000 0806		00000000	2786+	VL v21, 0(R1)	use v21 to test decoder
00004054	E310 5018 0014		00000018	2787+	LGF R1, V2ADDR	load v2 source
0000405A	E761 0000 0806		00000000	2788+	VL v22, 0(R1)	use v22 to test decoder
00004060	E310 501C 0014		0000001C	2789+	LGF R1, V3ADDR	load v3 source
00004066	E771 0000 0806		00000000	2790+	VL v23, 0(R1)	use v23 to test decoder
0000406C	E756 70FA 2E72			2791+	VERIM V21, V22, V23, 250, 2	test instruction
00004072	E750 5030 080E		00004030	2792+	VST V21, V1064	save v1 output
00004078	07FB			2793+	BR R11	return
0000407C				2794+RE64	DC OF	xl16 expected result
0000407C				2795+	DROP R5	
0000407C	00000000 04040404			2796	DC XL16' 0000000004040404 080808080C0C0C0C'	result t
00004084	08080808 0C0C0C0C					
0000408C	00010203 04050607			2797	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004094	08090A0B 0C0D0E0F					
0000409C	00010203 04050607			2798	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000040A4	08090A0B 0C0D0E0F					
000040AC	C3C3C3C3 C3C3C3C3			2799	DC XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000040B4	C3C3C3C3 C3C3C3C3					
				2800		
000040C0				2801	VRI_D VERIM, 248, 2	248-8 right
000040C0		000040C0		2802+	DS OFD	
000040C0	00004108			2803+	USING *, R5	base for test data and test routine
000040C4	0041			2804+T65	DC A(X65)	address of test routine
000040C6	00			2805+	DC H' 65'	test number
000040C6	00			2806+	DC X' 00'	
000040C7	F8			2807+	DC HL1' 248'	i4 field
000040C8	02			2808+	DC HL1' 2'	m5 field
000040C9	E5C5D9C9 D4404040			2809+	DC CL8' VERIM	instruction name
000040D4	0000414C			2810+	DC A(RE65+16)	address of v1 source
000040D8	0000415C			2811+	DC A(RE65+32)	address of v2 source
000040DC	0000416C			2812+	DC A(RE65+48)	address of v3 source
000040E0	00000010			2813+	DC A(16)	result length
000040E4	0000413C			2814+REA65	DC A(RE65)	result address
000040E8	00000000 00000000			2815+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				2837 *Doubleword		
				2838	VRI_D VERIM, 0, 3	
00004180				2839+	DS OFD	
00004180		00004180		2840+	USING *, R5	base for test data and test routine
00004180	000041C8			2841+T66	DC A(X66)	address of test routine
00004184	0042			2842+	DC H' 66'	test number
00004186	00			2843+	DC X' 00'	
00004187	00			2844+	DC HL1' 0'	i4 field
00004188	03			2845+	DC HL1' 3'	m5 field
00004189	E5C5D9C9 D4404040			2846+	DC CL8' VERIM	instruction name
00004194	0000420C			2847+	DC A(RE66+16)	address of v1 source
00004198	0000421C			2848+	DC A(RE66+32)	address of v2 source
0000419C	0000422C			2849+	DC A(RE66+48)	address of v3 source
000041A0	00000010			2850+	DC A(16)	result length
000041A4	000041FC			2851+REA66	DC A(RE66)	result address
000041A8	00000000 00000000			2852+	DS FD	gap
000041B0	00000000 00000000			2853+V1066	DS XL16	V1 output
000041B8	00000000 00000000					
000041C0	00000000 00000000			2854+	DS FD	gap
				2855+*		
000041C8				2856+X66	DS OF	
000041C8	E310 5014 0014		00000014	2857+	LGF R1, V1ADDR	load v1 source
000041CE	E751 0000 0806		00000000	2858+	VL v21, 0(R1)	use v21 to test decoder
000041D4	E310 5018 0014		00000018	2859+	LGF R1, V2ADDR	load v2 source
000041DA	E761 0000 0806		00000000	2860+	VL v22, 0(R1)	use v22 to test decoder
000041E0	E310 501C 0014		0000001C	2861+	LGF R1, V3ADDR	load v3 source
000041E6	E771 0000 0806		00000000	2862+	VL v23, 0(R1)	use v23 to test decoder
000041EC	E756 7000 3E72			2863+	VERIM V21, V22, V23, 0, 3	test instruction
000041F2	E750 5030 080E		000041B0	2864+	VST V21, V1066	save v1 output
000041F8	07FB			2865+	BR R11	return
000041FC				2866+RE66	DC OF	xl16 expected result
000041FC				2867+	DROP R5	
000041FC	00010203 04050607			2868	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	result t
00004204	08090A0B 0C0D0E0F					
0000420C	00010203 04050607			2869	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004214	08090A0B 0C0D0E0F					
0000421C	00010203 04050607			2870	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00004224	08090A0B 0C0D0E0F					
0000422C	00000000 00000000			2871	DC XL16' 0000000000000000 0000000000000000'	v3
00004234	00000000 00000000					
				2872		
				2873	VRI_D VERIM, 1, 3	
00004240				2874+	DS OFD	
00004240		00004240		2875+	USING *, R5	base for test data and test routine
00004240	00004288			2876+T67	DC A(X67)	address of test routine
00004244	0043			2877+	DC H' 67'	test number
00004246	00			2878+	DC X' 00'	
00004247	01			2879+	DC HL1' 1'	i4 field
00004248	03			2880+	DC HL1' 3'	m5 field
00004249	E5C5D9C9 D4404040			2881+	DC CL8' VERIM	instruction name
00004254	000042CC			2882+	DC A(RE67+16)	address of v1 source
00004258	000042DC			2883+	DC A(RE67+32)	address of v2 source
0000425C	000042EC			2884+	DC A(RE67+48)	address of v3 source
00004260	00000010			2885+	DC A(16)	result length
00004264	000042BC			2886+REA67	DC A(RE67)	result address
00004268	00000000 00000000			2887+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004270	00000000 00000000			2888+V1067	DS	XL16	V1 output
00004278	00000000 00000000						
00004280	00000000 00000000			2889+ 2890+*	DS	FD	gap
00004288				2891+X67	DS	OF	
00004288	E310 5014 0014		00000014	2892+	LGF	R1, V1ADDR	load v1 source
0000428E	E751 0000 0806		00000000	2893+	VL	v21, 0(R1)	use v21 to test decoder
00004294	E310 5018 0014		00000018	2894+	LGF	R1, V2ADDR	load v2 source
0000429A	E761 0000 0806		00000000	2895+	VL	v22, 0(R1)	use v22 to test decoder
000042A0	E310 501C 0014		0000001C	2896+	LGF	R1, V3ADDR	load v3 source
000042A6	E771 0000 0806		00000000	2897+	VL	v23, 0(R1)	use v23 to test decoder
000042AC	E756 7001 3E72			2898+	VERIM	V21, V22, V23, 1, 3	test instruction
000042B2	E750 5030 080E		00004270	2899+	VST	V21, V1067	save v1 output
000042B8	07FB			2900+	BR	R11	return
000042BC				2901+RE67	DC	OF	xl16 expected result
000042BC				2902+	DROP	R5	
000042BC	00020002 04060406			2903	DC	XL16' 0002000204060406 080A080A0C0E0C0E'	result t
000042C4	080A080A 0C0E0C0E						
000042CC	00010203 04050607			2904	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
000042D4	08090A0B 0C0D0E0F						
000042DC	00010203 04050607			2905	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000042E4	08090A0B 0C0D0E0F						
000042EC	C3C3C3C3 C3C3C3C3			2906	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000042F4	C3C3C3C3 C3C3C3C3						
				2907			
				2908	VRI_D	VERIM, 2, 3	
00004300				2909+	DS	OFD	
00004300		00004300		2910+	USING	*, R5	base for test data and test routine
00004300	00004348			2911+T68	DC	A(X68)	address of test routine
00004304	0044			2912+	DC	H' 68'	test number
00004306	00			2913+	DC	X' 00'	
00004307	02			2914+	DC	HL1' 2'	i4 field
00004308	03			2915+	DC	HL1' 3'	m5 field
00004309	E5C5D9C9 D4404040			2916+	DC	CL8' VERIM	instruction name
00004314	0000438C			2917+	DC	A(RE68+16)	address of v1 source
00004318	0000439C			2918+	DC	A(RE68+32)	address of v2 source
0000431C	000043AC			2919+	DC	A(RE68+48)	address of v3 source
00004320	00000010			2920+	DC	A(16)	result length
00004324	0000437C			2921+REA68	DC	A(RE68)	result address
00004328	00000000 00000000			2922+	DS	FD	gap
00004330	00000000 00000000			2923+V1068	DS	XL16	V1 output
00004338	00000000 00000000						
00004340	00000000 00000000			2924+ 2925+*	DS	FD	gap
00004348				2926+X68	DS	OF	
00004348	E310 5014 0014		00000014	2927+	LGF	R1, V1ADDR	load v1 source
0000434E	E751 0000 0806		00000000	2928+	VL	v21, 0(R1)	use v21 to test decoder
00004354	E310 5018 0014		00000018	2929+	LGF	R1, V2ADDR	load v2 source
0000435A	E761 0000 0806		00000000	2930+	VL	v22, 0(R1)	use v22 to test decoder
00004360	E310 501C 0014		0000001C	2931+	LGF	R1, V3ADDR	load v3 source
00004366	E771 0000 0806		00000000	2932+	VL	v23, 0(R1)	use v23 to test decoder
0000436C	E756 7002 3E72			2933+	VERIM	V21, V22, V23, 2, 3	test instruction
00004372	E750 5030 080E		00004330	2934+	VST	V21, V1068	save v1 output
00004378	07FB			2935+	BR	R11	return
0000437C				2936+RE68	DC	OF	xl16 expected result
0000437C				2937+	DROP	R5	

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000437C	00000000 04040404			2938	DC	XL16' 0000000004040404 080808080C0C0C0C'	result
00004384	08080808 0C0C0C0C						
0000438C	00010203 04050607			2939	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004394	08090A0B 0C0D0E0F						
0000439C	00010203 04050607			2940	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000043A4	08090A0B 0C0D0E0F						
000043AC	C3C3C3C3 C3C3C3C3			2941	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000043B4	C3C3C3C3 C3C3C3C3						
				2942			
				2943	VRI_D	VERIM 5, 3	
000043C0				2944+	DS	OFD	
000043C0		000043C0		2945+	USING	*, R5	base for test data and test routine
000043C0	00004408			2946+T69	DC	A(X69)	address of test routine
000043C4	0045			2947+	DC	H' 69'	test number
000043C6	00			2948+	DC	X' 00'	
000043C7	05			2949+	DC	HL1' 5'	i4 field
000043C8	03			2950+	DC	HL1' 3'	m5 field
000043C9	E5C5D9C9 D4404040			2951+	DC	CL8' VERIM	instruction name
000043D4	0000444C			2952+	DC	A(RE69+16)	address of v1 source
000043D8	0000445C			2953+	DC	A(RE69+32)	address of v2 source
000043DC	0000446C			2954+	DC	A(RE69+48)	address of v3 source
000043E0	00000010			2955+	DC	A(16)	result length
000043E4	0000443C			2956+REA69	DC	A(RE69)	result address
000043E8	00000000 00000000			2957+	DS	FD	gap
000043F0	00000000 00000000			2958+V1069	DS	XL16	V1 output
000043F8	00000000 00000000						
00004400	00000000 00000000			2959+	DS	FD	gap
				2960+*			
00004408				2961+X69	DS	OF	
00004408	E310 5014 0014		00000014	2962+	LGF	R1, V1ADDR	load v1 source
0000440E	E751 0000 0806		00000000	2963+	VL	v21, 0(R1)	use v21 to test decoder
00004414	E310 5018 0014		00000018	2964+	LGF	R1, V2ADDR	load v2 source
0000441A	E761 0000 0806		00000000	2965+	VL	v22, 0(R1)	use v22 to test decoder
00004420	E310 501C 0014		0000001C	2966+	LGF	R1, V3ADDR	load v3 source
00004426	E771 0000 0806		00000000	2967+	VL	v23, 0(R1)	use v23 to test decoder
0000442C	E756 7005 3E72			2968+	VERIM	V21, V22, V23, 5, 3	test instruction
00004432	E750 5030 080E		000043F0	2969+	VST	V21, V1069	save v1 output
00004438	07FB			2970+	BR	R11	return
0000443C				2971+RE69	DC	OF	xl16 expected result
0000443C				2972+	DROP	R5	
0000443C	00004040 8484C4C4			2973	DC	XL16' 000040408484C4C4 090949498D8DCDCD'	result
00004444	09094949 8D8DCDCD						
0000444C	00010203 04050607			2974	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004454	08090A0B 0C0D0E0F						
0000445C	00010203 04050607			2975	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00004464	08090A0B 0C0D0E0F						
0000446C	C3C3C3C3 C3C3C3C3			2976	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00004474	C3C3C3C3 C3C3C3C3						
				2977			
				2978	VRI_D	VERIM 7, 3	
00004480				2979+	DS	OFD	
00004480		00004480		2980+	USING	*, R5	base for test data and test routine
00004480	000044C8			2981+T70	DC	A(X70)	address of test routine
00004484	0046			2982+	DC	H' 70'	test number
00004486	00			2983+	DC	X' 00'	
00004487	07			2984+	DC	HL1' 7'	i4 field

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
00004488	03			2985+	DC	HL1' 3'	m5 field
00004489	E5C5D9C9 D4404040			2986+	DC	CL8' VERIM	instruction name
00004494	0000450C			2987+	DC	A(RE70+16)	address of v1 source
00004498	0000451C			2988+	DC	A(RE70+32)	address of v2 source
0000449C	0000452C			2989+	DC	A(RE70+48)	address of v3 source
000044A0	00000010			2990+	DC	A(16)	result length
000044A4	000044FC			2991+REA70	DC	A(RE70)	result address
000044A8	00000000 00000000			2992+	DS	FD	gap
000044B0	00000000 00000000			2993+V1070	DS	XL16	V1 output
000044B8	00000000 00000000						
000044C0	00000000 00000000			2994+	DS	FD	gap
				2995+*			
000044C8				2996+X70	DS	0F	
000044C8	E310 5014 0014		00000014	2997+	LGF	R1, V1ADDR	load v1 source
000044CE	E751 0000 0806		00000000	2998+	VL	v21, 0(R1)	use v21 to test decoder
000044D4	E310 5018 0014		00000018	2999+	LGF	R1, V2ADDR	load v2 source
000044DA	E761 0000 0806		00000000	3000+	VL	v22, 0(R1)	use v22 to test decoder
000044E0	E310 501C 0014		0000001C	3001+	LGF	R1, V3ADDR	load v3 source
000044E6	E771 0000 0806		00000000	3002+	VL	v23, 0(R1)	use v23 to test decoder
000044EC	E756 7007 3E72			3003+	VERIM	V21, V22, V23, 7, 3	test instruction
000044F2	E750 5030 080E		000044B0	3004+	VST	V21, V1070	save v1 output
000044F8	07FB			3005+	BR	R11	return
000044FC				3006+RE70	DC	0F	xl16 expected result
000044FC				3007+	DROP	R5	
000044FC	00810182 06870784			3008	DC	XL16' 0081018206870784 0889098A0E8F0F8C'	result t
00004504	0889098A 0E8F0F8C						
0000450C	00010203 04050607			3009	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004514	08090A0B 0C0D0E0F						
0000451C	00010203 04050607			3010	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00004524	08090A0B 0C0D0E0F						
0000452C	C3C3C3C3 C3C3C3C3			3011	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00004534	C3C3C3C3 C3C3C3C3						
				3012			
				3013	VRI_D	VERIM, 255, 3	255->1 right
00004540				3014+	DS	0FD	
00004540		00004540		3015+	USING	*, R5	base for test data and test routine
00004540	00004588			3016+T71	DC	A(X71)	address of test routine
00004544	0047			3017+	DC	H' 71'	test number
00004546	00			3018+	DC	X' 00'	
00004547	FF			3019+	DC	HL1' 255'	i4 field
00004548	03			3020+	DC	HL1' 3'	m5 field
00004549	E5C5D9C9 D4404040			3021+	DC	CL8' VERIM	instruction name
00004554	000045CC			3022+	DC	A(RE71+16)	address of v1 source
00004558	000045DC			3023+	DC	A(RE71+32)	address of v2 source
0000455C	000045EC			3024+	DC	A(RE71+48)	address of v3 source
00004560	00000010			3025+	DC	A(16)	result length
00004564	000045BC			3026+REA71	DC	A(RE71)	result address
00004568	00000000 00000000			3027+	DS	FD	gap
00004570	00000000 00000000			3028+V1071	DS	XL16	V1 output
00004578	00000000 00000000						
00004580	00000000 00000000			3029+	DS	FD	gap
				3030+*			
00004588				3031+X71	DS	0F	
00004588	E310 5014 0014		00000014	3032+	LGF	R1, V1ADDR	load v1 source
0000458E	E751 0000 0806		00000000	3033+	VL	v21, 0(R1)	use v21 to test decoder
00004594	E310 5018 0014		00000018	3034+	LGF	R1, V2ADDR	load v2 source

LOC	OBJECT CODE	ADDR1	ADDR2	STMT			
0000459A	E761 0000 0806		00000000	3035+	VL	v22, 0(R1)	use v22 to test decoder
000045A0	E310 501C 0014		0000001C	3036+	LGF	R1, V3ADDR	load v3 source
000045A6	E771 0000 0806		00000000	3037+	VL	v23, 0(R1)	use v23 to test decoder
000045AC	E756 70FF 3E72			3038+	VERIM	V21, V22, V23, 255, 3	test instruction
000045B2	E750 5030 080E		00004570	3039+	VST	V21, V1071	save v1 output
000045B8	07FB			3040+	BR	R11	return
000045BC				3041+RE71	DC	0F	xl16 expected result
000045BC				3042+	DROP	R5	
000045BC	80008101 86068707			3043	DC	XL16' 8000810186068707 880889098E0E8F0F'	result t
000045C4	88088909 8E0E8F0F						
000045CC	00010203 04050607			3044	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
000045D4	08090A0B 0C0D0E0F						
000045DC	00010203 04050607			3045	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000045E4	08090A0B 0C0D0E0F						
000045EC	C3C3C3C3 C3C3C3C3			3046	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000045F4	C3C3C3C3 C3C3C3C3						
				3047			
00004600				3048	VRI_D	VERIM, 254, 3	254->2 right
00004600		00004600		3049+	DS	0FD	
00004600	00004648			3050+	USING	*, R5	base for test data and test routine
00004604	0048			3051+T72	DC	A(X72)	address of test routine
00004606	00			3052+	DC	H' 72'	test number
00004606	00			3053+	DC	X' 00'	
00004607	FE			3054+	DC	HL1' 254'	i4 field
00004608	03			3055+	DC	HL1' 3'	m5 field
00004609	E5C5D9C9 D4404040			3056+	DC	CL8' VERIM	instruction name
00004614	0000468C			3057+	DC	A(RE72+16)	address of v1 source
00004618	0000469C			3058+	DC	A(RE72+32)	address of v2 source
0000461C	000046AC			3059+	DC	A(RE72+48)	address of v3 source
00004620	00000010			3060+	DC	A(16)	result length
00004624	0000467C			3061+REA72	DC	A(RE72)	result address
00004628	00000000 00000000			3062+	DS	FD	gap
00004630	00000000 00000000			3063+V1072	DS	XL16	V1 output
00004638	00000000 00000000						
00004640	00000000 00000000			3064+	DS	FD	gap
				3065+*			
00004648				3066+X72	DS	0F	
00004648	E310 5014 0014		00000014	3067+	LGF	R1, V1ADDR	load v1 source
0000464E	E751 0000 0806		00000000	3068+	VL	v21, 0(R1)	use v21 to test decoder
00004654	E310 5018 0014		00000018	3069+	LGF	R1, V2ADDR	load v2 source
0000465A	E761 0000 0806		00000000	3070+	VL	v22, 0(R1)	use v22 to test decoder
00004660	E310 501C 0014		0000001C	3071+	LGF	R1, V3ADDR	load v3 source
00004666	E771 0000 0806		00000000	3072+	VL	v23, 0(R1)	use v23 to test decoder
0000466C	E756 70FE 3E72			3073+	VERIM	V21, V22, V23, 254, 3	test instruction
00004672	E750 5030 080E		00004630	3074+	VST	V21, V1072	save v1 output
00004678	07FB			3075+	BR	R11	return
0000467C				3076+RE72	DC	0F	xl16 expected result
0000467C				3077+	DROP	R5	
0000467C	C0004080 C5054585			3078	DC	XL16' C0004080C5054585 CA0A4A8ACF0F4F8F'	result t
00004684	CA0A4A8A CF0F4F8F						
0000468C	00010203 04050607			3079	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004694	08090A0B 0C0D0E0F						
0000469C	00010203 04050607			3080	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
000046A4	08090A0B 0C0D0E0F						
000046AC	C3C3C3C3 C3C3C3C3			3081	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
000046B4	C3C3C3C3 C3C3C3C3						

LOC	OBJECT CODE	ADDR1	ADDR2	STMT		
				3082		
				3083	VRI_D VERIM, 250, 3	250->6 right
000046C0				3084+	DS OFD	
000046C0		000046C0		3085+	USING *, R5	base for test data and test routine
000046C0	00004708			3086+T73	DC A(X73)	address of test routine
000046C4	0049			3087+	DC H' 73'	test number
000046C6	00			3088+	DC X' 00'	
000046C7	FA			3089+	DC HL1' 250'	i4 field
000046C8	03			3090+	DC HL1' 3'	m5 field
000046C9	E5C5D9C9 D4404040			3091+	DC CL8' VERIM	instruction name
000046D4	0000474C			3092+	DC A(RE73+16)	address of v1 source
000046D8	0000475C			3093+	DC A(RE73+32)	address of v2 source
000046DC	0000476C			3094+	DC A(RE73+48)	address of v3 source
000046E0	00000010			3095+	DC A(16)	result length
000046E4	0000473C			3096+REA73	DC A(RE73)	result address
000046E8	00000000 00000000			3097+	DS FD	gap
000046F0	00000000 00000000			3098+V1073	DS XL16	V1 output
000046F8	00000000 00000000					
00004700	00000000 00000000			3099+	DS FD	gap
				3100+*		
00004708				3101+X73	DS OF	
00004708	E310 5014 0014		00000014	3102+	LGF R1, V1ADDR	load v1 source
0000470E	E751 0000 0806		00000000	3103+	VL v21, 0(R1)	use v21 to test decoder
00004714	E310 5018 0014		00000018	3104+	LGF R1, V2ADDR	load v2 source
0000471A	E761 0000 0806		00000000	3105+	VL v22, 0(R1)	use v22 to test decoder
00004720	E310 501C 0014		0000001C	3106+	LGF R1, V3ADDR	load v3 source
00004726	E771 0000 0806		00000000	3107+	VL v23, 0(R1)	use v23 to test decoder
0000472C	E756 70FA 3E72			3108+	VERIM V21, V22, V23, 250, 3	test instruction
00004732	E750 5030 080E		000046F0	3109+	VST V21, V1073	save v1 output
00004738	07FB			3110+	BR R11	return
0000473C				3111+RE73	DC OF	xl16 expected result
0000473C				3112+	DROP R5	
0000473C	00000000 04040404			3113	DC XL16' 0000000004040404 080808080C0C0C0C'	result t
00004744	08080808 0C0C0C0C					
0000474C	00010203 04050607			3114	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v1
00004754	08090A0B 0C0D0E0F					
0000475C	00010203 04050607			3115	DC XL16' 0001020304050607 08090A0B0C0D0E0F'	v2
00004764	08090A0B 0C0D0E0F					
0000476C	C3C3C3C3 C3C3C3C3			3116	DC XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3
00004774	C3C3C3C3 C3C3C3C3					
				3117		
00004780				3118	VRI_D VERIM, 248, 3	248-8 right
00004780		00004780		3119+	DS OFD	
00004780	000047C8			3120+	USING *, R5	base for test data and test routine
00004784	004A			3121+T74	DC A(X74)	address of test routine
00004786	00			3122+	DC H' 74'	test number
00004787	F8			3123+	DC X' 00'	
00004788	03			3124+	DC HL1' 248'	i4 field
00004789	E5C5D9C9 D4404040			3125+	DC HL1' 3'	m5 field
00004794	0000480C			3126+	DC CL8' VERIM	instruction name
00004798	0000481C			3127+	DC A(RE74+16)	address of v1 source
0000479C	0000482C			3128+	DC A(RE74+32)	address of v2 source
000047A0	00000010			3129+	DC A(RE74+48)	address of v3 source
000047A4	000047FC			3130+	DC A(16)	result length
000047A8	00000000 00000000			3131+REA74	DC A(RE74)	result address
				3132+	DS FD	gap

LOC	OBJECT CODE	ADDR1	ADDR2	STMT				
000047B0	00000000 00000000			3133+V1074	DS	XL16	V1 output	
000047B8	00000000 00000000							
000047C0	00000000 00000000			3134+	DS	FD	gap	
				3135+*				
000047C8				3136+X74	DS	0F		
000047C8	E310 5014 0014		00000014	3137+	LGF	R1, V1ADDR	load v1 source	
000047CE	E751 0000 0806		00000000	3138+	VL	v21, 0(R1)	use v21 to test decoder	
000047D4	E310 5018 0014		00000018	3139+	LGF	R1, V2ADDR	load v2 source	
000047DA	E761 0000 0806		00000000	3140+	VL	v22, 0(R1)	use v22 to test decoder	
000047E0	E310 501C 0014		0000001C	3141+	LGF	R1, V3ADDR	load v3 source	
000047E6	E771 0000 0806		00000000	3142+	VL	v23, 0(R1)	use v23 to test decoder	
000047EC	E756 70F8 3E72			3143+	VERIM	V21, V22, V23, 248, 3	test instruction	
000047F2	E750 5030 080E		000047B0	3144+	VST	V21, V1074	save v1 output	
000047F8	07FB			3145+	BR	R11	return	
000047FC				3146+RE74	DC	0F	xl16 expected result	
000047FC				3147+	DROP	R5		
000047FC	03000102 07040506			3148	DC	XL16' 0300010207040506 0B08090A0F0C0D0E'	result t	
00004804	0B08090A 0F0C0D0E							
0000480C	00010203 04050607			3149	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v1	
00004814	08090A0B 0C0D0E0F							
0000481C	00010203 04050607			3150	DC	XL16' 0001020304050607 08090A0B0C0D0E0F'	v2	
00004824	08090A0B 0C0D0E0F							
0000482C	C3C3C3C3 C3C3C3C3			3151	DC	XL16' C3C3C3C3C3C3C3C3 C3C3C3C3C3C3C3C3'	v3	
00004834	C3C3C3C3 C3C3C3C3							
				3152				
0000483C	00000000			3153	DC	F' 0'	END OF TABLE	
00004840	00000000			3154	DC	F' 0'		
				3155 *				
				3156 *	table of pointers to individual load test			
				3157 *				
00004844				3158 E7TESTS	DS	0F		
				3159	PTTABLE			
00004844				3160+TTABLE	DS	0F		
00004844	000010C0			3161+	DC	A(T1)		
00004848	00001180			3162+	DC	A(T2)		
0000484C	00001240			3163+	DC	A(T3)		
00004850	00001300			3164+	DC	A(T4)		
00004854	000013C0			3165+	DC	A(T5)		
00004858	00001480			3166+	DC	A(T6)		
0000485C	00001540			3167+	DC	A(T7)		
00004860	00001600			3168+	DC	A(T8)		
00004864	000016C0			3169+	DC	A(T9)		
00004868	00001780			3170+	DC	A(T10)		
0000486C	00001840			3171+	DC	A(T11)		
00004870	00001900			3172+	DC	A(T12)		
00004874	000019C0			3173+	DC	A(T13)		
00004878	00001A80			3174+	DC	A(T14)		
0000487C	00001B40			3175+	DC	A(T15)		
00004880	00001C00			3176+	DC	A(T16)		
00004884	00001CC0			3177+	DC	A(T17)		
00004888	00001D80			3178+	DC	A(T18)		
0000488C	00001E40			3179+	DC	A(T19)		
00004890	00001F00			3180+	DC	A(T20)		
00004894	00001FC0			3181+	DC	A(T21)		
00004898	00002080			3182+	DC	A(T22)		
0000489C	00002140			3183+	DC	A(T23)		

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
000048A0	00002200			3184+	DC A(T24)
000048A4	000022C0			3185+	DC A(T25)
000048A8	00002380			3186+	DC A(T26)
000048AC	00002440			3187+	DC A(T27)
000048B0	00002500			3188+	DC A(T28)
000048B4	000025C0			3189+	DC A(T29)
000048B8	00002680			3190+	DC A(T30)
000048BC	00002740			3191+	DC A(T31)
000048C0	00002800			3192+	DC A(T32)
000048C4	000028C0			3193+	DC A(T33)
000048C8	00002980			3194+	DC A(T34)
000048CC	00002A40			3195+	DC A(T35)
000048D0	00002B00			3196+	DC A(T36)
000048D4	00002BC0			3197+	DC A(T37)
000048D8	00002C80			3198+	DC A(T38)
000048DC	00002D40			3199+	DC A(T39)
000048E0	00002E00			3200+	DC A(T40)
000048E4	00002EC0			3201+	DC A(T41)
000048E8	00002F80			3202+	DC A(T42)
000048EC	00003040			3203+	DC A(T43)
000048F0	00003100			3204+	DC A(T44)
000048F4	000031C0			3205+	DC A(T45)
000048F8	00003280			3206+	DC A(T46)
000048FC	00003340			3207+	DC A(T47)
00004900	00003400			3208+	DC A(T48)
00004904	000034C0			3209+	DC A(T49)
00004908	00003580			3210+	DC A(T50)
0000490C	00003640			3211+	DC A(T51)
00004910	00003700			3212+	DC A(T52)
00004914	000037C0			3213+	DC A(T53)
00004918	00003880			3214+	DC A(T54)
0000491C	00003940			3215+	DC A(T55)
00004920	00003A00			3216+	DC A(T56)
00004924	00003AC0			3217+	DC A(T57)
00004928	00003B80			3218+	DC A(T58)
0000492C	00003C40			3219+	DC A(T59)
00004930	00003D00			3220+	DC A(T60)
00004934	00003DC0			3221+	DC A(T61)
00004938	00003E80			3222+	DC A(T62)
0000493C	00003F40			3223+	DC A(T63)
00004940	00004000			3224+	DC A(T64)
00004944	000040C0			3225+	DC A(T65)
00004948	00004180			3226+	DC A(T66)
0000494C	00004240			3227+	DC A(T67)
00004950	00004300			3228+	DC A(T68)
00004954	000043C0			3229+	DC A(T69)
00004958	00004480			3230+	DC A(T70)
0000495C	00004540			3231+	DC A(T71)
00004960	00004600			3232+	DC A(T72)
00004964	000046C0			3233+	DC A(T73)
00004968	00004780			3234+	DC A(T74)
				3235+*	
0000496C	00000000			3236+	DC A(0) END OF TABLE
00004970	00000000			3237+	DC A(0)
				3238	
00004974	00000000			3239	DC F' 0' END OF TABLE

LOC	OBJECT CODE	ADDR1	ADDR2	STMT	
				3242	*****
				3243	* Register equates
				3244	*****
		00000000	00000001	3246 R0	EQU 0
		00000001	00000001	3247 R1	EQU 1
		00000002	00000001	3248 R2	EQU 2
		00000003	00000001	3249 R3	EQU 3
		00000004	00000001	3250 R4	EQU 4
		00000005	00000001	3251 R5	EQU 5
		00000006	00000001	3252 R6	EQU 6
		00000007	00000001	3253 R7	EQU 7
		00000008	00000001	3254 R8	EQU 8
		00000009	00000001	3255 R9	EQU 9
		0000000A	00000001	3256 R10	EQU 10
		0000000B	00000001	3257 R11	EQU 11
		0000000C	00000001	3258 R12	EQU 12
		0000000D	00000001	3259 R13	EQU 13
		0000000E	00000001	3260 R14	EQU 14
		0000000F	00000001	3261 R15	EQU 15
				3263	*****
				3264	* Register equates
				3265	*****
		00000000	00000001	3267 V0	EQU 0
		00000001	00000001	3268 V1	EQU 1
		00000002	00000001	3269 V2	EQU 2
		00000003	00000001	3270 V3	EQU 3
		00000004	00000001	3271 V4	EQU 4
		00000005	00000001	3272 V5	EQU 5
		00000006	00000001	3273 V6	EQU 6
		00000007	00000001	3274 V7	EQU 7
		00000008	00000001	3275 V8	EQU 8
		00000009	00000001	3276 V9	EQU 9
		0000000A	00000001	3277 V10	EQU 10
		0000000B	00000001	3278 V11	EQU 11
		0000000C	00000001	3279 V12	EQU 12
		0000000D	00000001	3280 V13	EQU 13
		0000000E	00000001	3281 V14	EQU 14
		0000000F	00000001	3282 V15	EQU 15
		00000010	00000001	3283 V16	EQU 16
		00000011	00000001	3284 V17	EQU 17
		00000012	00000001	3285 V18	EQU 18
		00000013	00000001	3286 V19	EQU 19
		00000014	00000001	3287 V20	EQU 20
		00000015	00000001	3288 V21	EQU 21

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES																						
BEGIN	I	00000200	2	153	119	149	150	151																			
CTLR0	F	000004AC	4	356	163	164	165	166																			
DECNUM	C	00001080	16	409	263	265	272	274											279	281							
E7TEST	4	00000000	72	423	212																						
E7TESTS	F	00004844	4	3158	205																						
EDIT	X	00001054	18	404	264											273	280										
ENDTEST	U	0000031E	1	249	210																						
E0J	I	00000490	4	346	198											252											
E0JPSW	D	00000480	8	344	346																						
FAILCONT	U	0000030E	1	239																							
FAILED	F	00001000	4	384	241											250											
FAILMSG	U	0000030A	1	233	223																						
FAILPSW	D	00000498	8	348	350																						
FAILTEST	I	000004A8	4	350	253																						
FB0001	F	00000280	8	182	186											187	189										
I4	U	00000007	1	427	271																						
IMAGE	1	00000000	18812	0																							
K	U	00000400	1	368																369	370	371					
K64	U	00010000	1	370																							
M5	U	00000008	1	428																278							
MB	U	00100000	1	371																							
MSG	I	000003C8	4	306																197	289						
MSGCMD	C	00000416	9	336																319	320						
MSGMSG	C	0000041F	95	337																313	334	311					
MSGMVC	I	00000410	6	334	317																						
MSGOK	I	000003DE	2	315	312																						
MSGRET	I	000003FE	4	330	323											326											
MSGSAVE	F	00000404	4	333	309											330											
NEXTE7	U	000002D4	1	207	226	244																					
OPNAME	C	00000009	8	430	268																						
PAGE	U	00001000	1	369																							
PRT3	C	0000106A	18	407	264	265											266	273	274	275	280	281	282				
PRTI4	C	00001044	3	395	275																						
PRTLIN	C	00001008	16	390	399											288											
PRTLNG	U	0000004C	1	399	287																						
PRTM5	C	00001051	2	397	282																						
PRTNAME	C	00001033	8	393	268																						
PRTNUM	C	00001018	3	391	266																						
R0	U	00000000	1	3246	113											163	166	186	188	189	190	195	214	215	240	241	286
R1	U	00000001	1	3247	196											221	222	250	251	288	320	334	564	565	566	567	568
					569	599	600	601	602	603	604	638	639	640	641	642	643										
					673	674	675	676	677	678	708	709	710	711	712	713	743										
					744	745	746	747	748	778	779	780	781	782	783	813	814										
					815	816	817	818	848	849	850	851	852	853	883	884	885										
					886	887	888	918	919	920	921	922	923	955	956	957	958										
					959	960	990	991	992	993	994	995	1025	1026	1027	1028	1029										
					1030	1060	1061	1062	1063	1064	1065	1095	1096	1097	1098	1099	1100										
					1130	1131	1132	1133	1134	1135	1165	1166	1167	1168	1169	1170	1200										
					1201	1202	1203	1204	1205	1235	1236	1237	1238	1239	1240	1271	1272										
					1273	1274	1275	1276	1306	1307	1308	1309	1310	1311	1341	1342	1343										
					1344	1345	1346	1376	1377	1378	1379	1380	1381	1411	1412	1413	1414										
					1415	1416	1446	1447	1448	1449	1450	1451	1481	1482	1483	1484	1485										
					1486	1516	1517	1518	1519	1520	1521	1551	1552	1553	1554	1555	1556										
					1588	1589	1590	1591	1592	1593	1623	1624	1625	1626	1627	1628	1658										
					1659	1660	1661	1662	1663	1693	1694	1695	1696	1697	1698	1728	1729										

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
RE15	F	00001BBC	4	1069	1050	1051	1052	1054	
RE16	F	00001C7C	4	1104	1085	1086	1087	1089	
RE17	F	00001D3C	4	1139	1120	1121	1122	1124	
RE18	F	00001DFC	4	1174	1155	1156	1157	1159	
RE19	F	00001EBC	4	1209	1190	1191	1192	1194	
RE2	F	000011FC	4	608	589	590	591	593	
RE20	F	00001F7C	4	1244	1225	1226	1227	1229	
RE21	F	0000203C	4	1280	1261	1262	1263	1265	
RE22	F	000020FC	4	1315	1296	1297	1298	1300	
RE23	F	000021BC	4	1350	1331	1332	1333	1335	
RE24	F	0000227C	4	1385	1366	1367	1368	1370	
RE25	F	0000233C	4	1420	1401	1402	1403	1405	
RE26	F	000023FC	4	1455	1436	1437	1438	1440	
RE27	F	000024BC	4	1490	1471	1472	1473	1475	
RE28	F	0000257C	4	1525	1506	1507	1508	1510	
RE29	F	0000263C	4	1560	1541	1542	1543	1545	
RE3	F	000012BC	4	647	628	629	630	632	
RE30	F	000026FC	4	1597	1578	1579	1580	1582	
RE31	F	000027BC	4	1632	1613	1614	1615	1617	
RE32	F	0000287C	4	1667	1648	1649	1650	1652	
RE33	F	0000293C	4	1702	1683	1684	1685	1687	
RE34	F	000029FC	4	1737	1718	1719	1720	1722	
RE35	F	00002ABC	4	1772	1753	1754	1755	1757	
RE36	F	00002B7C	4	1807	1788	1789	1790	1792	
RE37	F	00002C3C	4	1842	1823	1824	1825	1827	
RE38	F	00002CFC	4	1877	1858	1859	1860	1862	
RE39	F	00002DBC	4	1916	1897	1898	1899	1901	
RE4	F	0000137C	4	682	663	664	665	667	
RE40	F	00002E7C	4	1951	1932	1933	1934	1936	
RE41	F	00002F3C	4	1986	1967	1968	1969	1971	
RE42	F	00002FFC	4	2021	2002	2003	2004	2006	
RE43	F	000030BC	4	2056	2037	2038	2039	2041	
RE44	F	0000317C	4	2091	2072	2073	2074	2076	
RE45	F	0000323C	4	2126	2107	2108	2109	2111	
RE46	F	000032FC	4	2161	2142	2143	2144	2146	
RE47	F	000033BC	4	2196	2177	2178	2179	2181	
RE48	F	0000347C	4	2233	2214	2215	2216	2218	
RE49	F	0000353C	4	2268	2249	2250	2251	2253	
RE5	F	0000143C	4	717	698	699	700	702	
RE50	F	000035FC	4	2303	2284	2285	2286	2288	
RE51	F	000036BC	4	2338	2319	2320	2321	2323	
RE52	F	0000377C	4	2373	2354	2355	2356	2358	
RE53	F	0000383C	4	2408	2389	2390	2391	2393	
RE54	F	000038FC	4	2443	2424	2425	2426	2428	
RE55	F	000039BC	4	2478	2459	2460	2461	2463	
RE56	F	00003A7C	4	2513	2494	2495	2496	2498	
RE57	F	00003B3C	4	2549	2530	2531	2532	2534	
RE58	F	00003BFC	4	2584	2565	2566	2567	2569	
RE59	F	00003CBC	4	2619	2600	2601	2602	2604	
RE6	F	000014FC	4	752	733	734	735	737	
RE60	F	00003D7C	4	2654	2635	2636	2637	2639	
RE61	F	00003E3C	4	2689	2670	2671	2672	2674	
RE62	F	00003EFC	4	2724	2705	2706	2707	2709	
RE63	F	00003FBC	4	2759	2740	2741	2742	2744	
RE64	F	0000407C	4	2794	2775	2776	2777	2779	
RE65	F	0000413C	4	2829	2810	2811	2812	2814	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES				
RE66	F	000041FC	4	2866	2847	2848	2849	2851	
RE67	F	000042BC	4	2901	2882	2883	2884	2886	
RE68	F	0000437C	4	2936	2917	2918	2919	2921	
RE69	F	0000443C	4	2971	2952	2953	2954	2956	
RE7	F	000015BC	4	787	768	769	770	772	
RE70	F	000044FC	4	3006	2987	2988	2989	2991	
RE71	F	000045BC	4	3041	3022	3023	3024	3026	
RE72	F	0000467C	4	3076	3057	3058	3059	3061	
RE73	F	0000473C	4	3111	3092	3093	3094	3096	
RE74	F	000047FC	4	3146	3127	3128	3129	3131	
RE8	F	0000167C	4	822	803	804	805	807	
RE9	F	0000173C	4	857	838	839	840	842	
REA1	A	000010E4	4	558					
REA10	A	000017A4	4	877					
REA11	A	00001864	4	912					
REA12	A	00001924	4	949					
REA13	A	000019E4	4	984					
REA14	A	00001AA4	4	1019					
REA15	A	00001B64	4	1054					
REA16	A	00001C24	4	1089					
REA17	A	00001CE4	4	1124					
REA18	A	00001DA4	4	1159					
REA19	A	00001E64	4	1194					
REA2	A	000011A4	4	593					
REA20	A	00001F24	4	1229					
REA21	A	00001FE4	4	1265					
REA22	A	000020A4	4	1300					
REA23	A	00002164	4	1335					
REA24	A	00002224	4	1370					
REA25	A	000022E4	4	1405					
REA26	A	000023A4	4	1440					
REA27	A	00002464	4	1475					
REA28	A	00002524	4	1510					
REA29	A	000025E4	4	1545					
REA3	A	00001264	4	632					
REA30	A	000026A4	4	1582					
REA31	A	00002764	4	1617					
REA32	A	00002824	4	1652					
REA33	A	000028E4	4	1687					
REA34	A	000029A4	4	1722					
REA35	A	00002A64	4	1757					
REA36	A	00002B24	4	1792					
REA37	A	00002BE4	4	1827					
REA38	A	00002CA4	4	1862					
REA39	A	00002D64	4	1901					
REA4	A	00001324	4	667					
REA40	A	00002E24	4	1936					
REA41	A	00002EE4	4	1971					
REA42	A	00002FA4	4	2006					
REA43	A	00003064	4	2041					
REA44	A	00003124	4	2076					
REA45	A	000031E4	4	2111					
REA46	A	000032A4	4	2146					
REA47	A	00003364	4	2181					
REA48	A	00003424	4	2218					
REA49	A	000034E4	4	2253					

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
REA5	A	000013E4	4	702		
REA50	A	000035A4	4	2288		
REA51	A	00003664	4	2323		
REA52	A	00003724	4	2358		
REA53	A	000037E4	4	2393		
REA54	A	000038A4	4	2428		
REA55	A	00003964	4	2463		
REA56	A	00003A24	4	2498		
REA57	A	00003AE4	4	2534		
REA58	A	00003BA4	4	2569		
REA59	A	00003C64	4	2604		
REA6	A	000014A4	4	737		
REA60	A	00003D24	4	2639		
REA61	A	00003DE4	4	2674		
REA62	A	00003EA4	4	2709		
REA63	A	00003F64	4	2744		
REA64	A	00004024	4	2779		
REA65	A	000040E4	4	2814		
REA66	A	000041A4	4	2851		
REA67	A	00004264	4	2886		
REA68	A	00004324	4	2921		
REA69	A	000043E4	4	2956		
REA7	A	00001564	4	772		
REA70	A	000044A4	4	2991		
REA71	A	00004564	4	3026		
REA72	A	00004624	4	3061		
REA73	A	000046E4	4	3096		
REA74	A	000047A4	4	3131		
REA8	A	00001624	4	807		
REA9	A	000016E4	4	842		
READDR	A	00000024	4	435	221	
REG2LOW	U	000000DD	1	374		
REG2PATT	U	AABBCCDD	1	373		
RELEN	A	00000020	4	434		
RPTDWSAV	D	000003B8	8	299	286	290
RPTERROR	I	0000032C	4	259	234	
RPTSAVE	F	000003AC	4	296	259	293
RPTSVR5	F	000003B0	4	297	260	292
SKL0001	U	0000004E	1	179	195	
SKT0001	C	0000022A	20	176	179	196
SVOLDPSW	U	00000140	0	115		
T1	A	000010C0	4	548	3161	
T10	A	00001780	4	867	3170	
T11	A	00001840	4	902	3171	
T12	A	00001900	4	939	3172	
T13	A	000019C0	4	974	3173	
T14	A	00001A80	4	1009	3174	
T15	A	00001B40	4	1044	3175	
T16	A	00001C00	4	1079	3176	
T17	A	00001CC0	4	1114	3177	
T18	A	00001D80	4	1149	3178	
T19	A	00001E40	4	1184	3179	
T2	A	00001180	4	583	3162	
T20	A	00001F00	4	1219	3180	
T21	A	00001FC0	4	1255	3181	
T22	A	00002080	4	1290	3182	

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES
T23	A	00002140	4	1325	3183
T24	A	00002200	4	1360	3184
T25	A	000022C0	4	1395	3185
T26	A	00002380	4	1430	3186
T27	A	00002440	4	1465	3187
T28	A	00002500	4	1500	3188
T29	A	000025C0	4	1535	3189
T3	A	00001240	4	622	3163
T30	A	00002680	4	1572	3190
T31	A	00002740	4	1607	3191
T32	A	00002800	4	1642	3192
T33	A	000028C0	4	1677	3193
T34	A	00002980	4	1712	3194
T35	A	00002A40	4	1747	3195
T36	A	00002B00	4	1782	3196
T37	A	00002BC0	4	1817	3197
T38	A	00002C80	4	1852	3198
T39	A	00002D40	4	1891	3199
T4	A	00001300	4	657	3164
T40	A	00002E00	4	1926	3200
T41	A	00002EC0	4	1961	3201
T42	A	00002F80	4	1996	3202
T43	A	00003040	4	2031	3203
T44	A	00003100	4	2066	3204
T45	A	000031C0	4	2101	3205
T46	A	00003280	4	2136	3206
T47	A	00003340	4	2171	3207
T48	A	00003400	4	2208	3208
T49	A	000034C0	4	2243	3209
T5	A	000013C0	4	692	3165
T50	A	00003580	4	2278	3210
T51	A	00003640	4	2313	3211
T52	A	00003700	4	2348	3212
T53	A	000037C0	4	2383	3213
T54	A	00003880	4	2418	3214
T55	A	00003940	4	2453	3215
T56	A	00003A00	4	2488	3216
T57	A	00003AC0	4	2524	3217
T58	A	00003B80	4	2559	3218
T59	A	00003C40	4	2594	3219
T6	A	00001480	4	727	3166
T60	A	00003D00	4	2629	3220
T61	A	00003DC0	4	2664	3221
T62	A	00003E80	4	2699	3222
T63	A	00003F40	4	2734	3223
T64	A	00004000	4	2769	3224
T65	A	000040C0	4	2804	3225
T66	A	00004180	4	2841	3226
T67	A	00004240	4	2876	3227
T68	A	00004300	4	2911	3228
T69	A	000043C0	4	2946	3229
T7	A	00001540	4	762	3167
T70	A	00004480	4	2981	3230
T71	A	00004540	4	3016	3231
T72	A	00004600	4	3051	3232
T73	A	000046C0	4	3086	3233

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
V1037	X	00002BF0	16	1829	1840												
V1038	X	00002CB0	16	1864	1875												
V1039	X	00002D70	16	1903	1914												
V104	X	00001330	16	669	680												
V1040	X	00002E30	16	1938	1949												
V1041	X	00002EF0	16	1973	1984												
V1042	X	00002FB0	16	2008	2019												
V1043	X	00003070	16	2043	2054												
V1044	X	00003130	16	2078	2089												
V1045	X	000031F0	16	2113	2124												
V1046	X	000032B0	16	2148	2159												
V1047	X	00003370	16	2183	2194												
V1048	X	00003430	16	2220	2231												
V1049	X	000034F0	16	2255	2266												
V105	X	000013F0	16	704	715												
V1050	X	000035B0	16	2290	2301												
V1051	X	00003670	16	2325	2336												
V1052	X	00003730	16	2360	2371												
V1053	X	000037F0	16	2395	2406												
V1054	X	000038B0	16	2430	2441												
V1055	X	00003970	16	2465	2476												
V1056	X	00003A30	16	2500	2511												
V1057	X	00003AF0	16	2536	2547												
V1058	X	00003BB0	16	2571	2582												
V1059	X	00003C70	16	2606	2617												
V106	X	000014B0	16	739	750												
V1060	X	00003D30	16	2641	2652												
V1061	X	00003DF0	16	2676	2687												
V1062	X	00003EB0	16	2711	2722												
V1063	X	00003F70	16	2746	2757												
V1064	X	00004030	16	2781	2792												
V1065	X	000040F0	16	2816	2827												
V1066	X	000041B0	16	2853	2864												
V1067	X	00004270	16	2888	2899												
V1068	X	00004330	16	2923	2934												
V1069	X	000043F0	16	2958	2969												
V107	X	00001570	16	774	785												
V1070	X	000044B0	16	2993	3004												
V1071	X	00004570	16	3028	3039												
V1072	X	00004630	16	3063	3074												
V1073	X	000046F0	16	3098	3109												
V1074	X	000047B0	16	3133	3144												
V108	X	00001630	16	809	820												
V109	X	000016F0	16	844	855												
V10OUTPUT	X	00000030	16	437	222												
V2	U	00000002	1	3269													
V20	U	00000014	1	3287													
V21	U	00000015	1	3288	565	570	571	600	605	606	639	644	645	674	679	680	709
					714	715	744	749	750	779	784	785	814	819	820	849	854
					855	884	889	890	919	924	925	956	961	962	991	996	997
					1026	1031	1032	1061	1066	1067	1096	1101	1102	1131	1136	1137	1166
					1171	1172	1201	1206	1207	1236	1241	1242	1272	1277	1278	1307	1312
					1313	1342	1347	1348	1377	1382	1383	1412	1417	1418	1447	1452	1453
					1482	1487	1488	1517	1522	1523	1552	1557	1558	1589	1594	1595	1624
					1629	1630	1659	1664	1665	1694	1699	1700	1729	1734	1735	1764	1769
					1770	1799	1804	1805	1834	1839	1840	1869	1874	1875	1908	1913	1914

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES												
					1943	1948	1949	1978	1983	1984	2013	2018	2019	2048	2053	2054	2083
					2088	2089	2118	2123	2124	2153	2158	2159	2188	2193	2194	2225	2230
					2231	2260	2265	2266	2295	2300	2301	2330	2335	2336	2365	2370	2371
					2400	2405	2406	2435	2440	2441	2470	2475	2476	2505	2510	2511	2541
					2546	2547	2576	2581	2582	2611	2616	2617	2646	2651	2652	2681	2686
					2687	2716	2721	2722	2751	2756	2757	2786	2791	2792	2821	2826	2827
					2858	2863	2864	2893	2898	2899	2928	2933	2934	2963	2968	2969	2998
					3003	3004	3033	3038	3039	3068	3073	3074	3103	3108	3109	3138	3143
					3144												
					567	570	602	605	641	644	676	679	711	714	746	749	781
V22	U	00000016	1	3289	784	816	819	851	854	886	889	921	924	958	961	993	996
					1028	1031	1063	1066	1098	1101	1133	1136	1168	1171	1203	1206	1238
					1241	1274	1277	1309	1312	1344	1347	1379	1382	1414	1417	1449	1452
					1484	1487	1519	1522	1554	1557	1591	1594	1626	1629	1661	1664	1696
					1699	1731	1734	1766	1769	1801	1804	1836	1839	1871	1874	1910	1913
					1945	1948	1980	1983	2015	2018	2050	2053	2085	2088	2120	2123	2155
					2158	2190	2193	2227	2230	2262	2265	2297	2300	2332	2335	2367	2370
					2402	2405	2437	2440	2472	2475	2507	2510	2543	2546	2578	2581	2613
					2616	2648	2651	2683	2686	2718	2721	2753	2756	2788	2791	2823	2826
					2860	2863	2895	2898	2930	2933	2965	2968	3000	3003	3035	3038	3070
V23	U	00000017	1	3290	3073	3105	3108	3140	3143								
					569	570	604	605	643	644	678	679	713	714	748	749	783
					784	818	819	853	854	888	889	923	924	960	961	995	996
					1030	1031	1065	1066	1100	1101	1135	1136	1170	1171	1205	1206	1240
					1241	1276	1277	1311	1312	1346	1347	1381	1382	1416	1417	1451	1452
					1486	1487	1521	1522	1556	1557	1593	1594	1628	1629	1663	1664	1698
					1699	1733	1734	1768	1769	1803	1804	1838	1839	1873	1874	1912	1913
					1947	1948	1982	1983	2017	2018	2052	2053	2087	2088	2122	2123	2157
					2158	2192	2193	2229	2230	2264	2265	2299	2300	2334	2335	2369	2370
					2404	2405	2439	2440	2474	2475	2509	2510	2545	2546	2580	2581	2615
					2616	2650	2651	2685	2686	2720	2721	2755	2756	2790	2791	2825	2826
					2862	2863	2897	2898	2932	2933	2967	2968	3002	3003	3037	3038	3072
					3073	3107	3108	3142	3143								
V24	U	00000018	1	3291													
V25	U	00000019	1	3292													
V26	U	0000001A	1	3293													
V27	U	0000001B	1	3294													
V28	U	0000001C	1	3295													
V29	U	0000001D	1	3296													
V2ADDR	A	00000018	4	432	566	601	640	675	710	745	780	815	850	885	920	957	992
					1027	1062	1097	1132	1167	1202	1237	1273	1308	1343	1378	1413	1448
					1483	1518	1553	1590	1625	1660	1695	1730	1765	1800	1835	1870	1909
					1944	1979	2014	2049	2084	2119	2154	2189	2226	2261	2296	2331	2366
					2401	2436	2471	2506	2542	2577	2612	2647	2682	2717	2752	2787	2822
					2859	2894	2929	2964	2999	3034	3069	3104	3139				
V3	U	00000003	1	3270													
V30	U	0000001E	1	3297													
V31	U	0000001F	1	3298													
V3ADDR	A	0000001C	4	433	568	603	642	677	712	747	782	817	852	887	922	959	994
					1029	1064	1099	1134	1169	1204	1239	1275	1310	1345	1380	1415	1450
					1485	1520	1555	1592	1627	1662	1697	1732	1767	1802	1837	1872	1911
					1946	1981	2016	2051	2086	2121	2156	2191	2228	2263	2298	2333	2368
					2403	2438	2473	2508	2544	2579	2614	2649	2684	2719	2754	2789	2824
					2861	2896	2931	2966	3001	3036	3071	3106	3141				
V4	U	00000004	1	3271													
V5	U	00000005	1	3272													

SYMBOL	TYPE	VALUE	LENGTH	DEFN	REFERENCES	
V6	U	00000006	1	3273		
V7	U	00000007	1	3274		
V8	U	00000008	1	3275		
V9	U	00000009	1	3276		
X0001	U	000002A8	1	185	173	186
X1	F	00001108	4	563	548	
X10	F	000017C8	4	882	867	
X11	F	00001888	4	917	902	
X12	F	00001948	4	954	939	
X13	F	00001A08	4	989	974	
X14	F	00001AC8	4	1024	1009	
X15	F	00001B88	4	1059	1044	
X16	F	00001C48	4	1094	1079	
X17	F	00001D08	4	1129	1114	
X18	F	00001DC8	4	1164	1149	
X19	F	00001E88	4	1199	1184	
X2	F	000011C8	4	598	583	
X20	F	00001F48	4	1234	1219	
X21	F	00002008	4	1270	1255	
X22	F	000020C8	4	1305	1290	
X23	F	00002188	4	1340	1325	
X24	F	00002248	4	1375	1360	
X25	F	00002308	4	1410	1395	
X26	F	000023C8	4	1445	1430	
X27	F	00002488	4	1480	1465	
X28	F	00002548	4	1515	1500	
X29	F	00002608	4	1550	1535	
X3	F	00001288	4	637	622	
X30	F	000026C8	4	1587	1572	
X31	F	00002788	4	1622	1607	
X32	F	00002848	4	1657	1642	
X33	F	00002908	4	1692	1677	
X34	F	000029C8	4	1727	1712	
X35	F	00002A88	4	1762	1747	
X36	F	00002B48	4	1797	1782	
X37	F	00002C08	4	1832	1817	
X38	F	00002CC8	4	1867	1852	
X39	F	00002D88	4	1906	1891	
X4	F	00001348	4	672	657	
X40	F	00002E48	4	1941	1926	
X41	F	00002F08	4	1976	1961	
X42	F	00002FC8	4	2011	1996	
X43	F	00003088	4	2046	2031	
X44	F	00003148	4	2081	2066	
X45	F	00003208	4	2116	2101	
X46	F	000032C8	4	2151	2136	
X47	F	00003388	4	2186	2171	
X48	F	00003448	4	2223	2208	
X49	F	00003508	4	2258	2243	
X5	F	00001408	4	707	692	
X50	F	000035C8	4	2293	2278	
X51	F	00003688	4	2328	2313	
X52	F	00003748	4	2363	2348	
X53	F	00003808	4	2398	2383	
X54	F	000038C8	4	2433	2418	
X55	F	00003988	4	2468	2453	

DESC	SYMBOL	SIZE	POS	ADDR
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Entry: 0

Image	IMAGE	18812	0000-497B	0000-497B
Regi on		18812	0000-497B	0000-497B
CSECT	ZVE7TST	18812	0000-497B	0000-497B

STMT	FILE NAME
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1	/home/tn529/sharedvfp/tests/zvector-e7-27-VERIM.asm
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** NO ERRORS FOUND **